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Rev. A

T-BERD 310
COMMUNICATIONS ANALYZER

USER'S GUIDE
for the
T-BERD 310-S OPTION

AUGUST 1995

This manual addresses the T-BERD310-S Option for use with Revision G or greater software.

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INTRODUCTION

1.1 OVERVIEW

The *T-BERD 310 User's Guide for the T-BERD 310-S SONET/ATM User Interface Option* offers an easy, direct method to setup and operate the T-BERD 310 within your network. It presents frequently used test setups in their entirety. Illustrations, notes, and step-by-step procedures make this guide a valuable tool for both new and experienced users.

This guide is designed for the user who needs to quickly know the basics about setting up and operating the T-BERD 310. If you are unfamiliar with the instrument, please refer to the *T-BERD 310 Reference Manual* for more detailed information. If you need additional help, call TTC Customer Service at (800) 638-2049.

1.2 T-BERD 310 OPTIONS

This guide contains applications for the following T-BERD 310 options. Options are identified at the beginning of the application. One or more of the options may be used in a single application.

- 310-1 DS1/DS0 Analyzer Option
- 310-2 E1 Drop Option
- 310-3 DS1 Insert Option
- 310-5 DS3 Jitter Option
- 310-6 IEEE-488 Option
- 310-9A Enhanced ESF/DS1 Timing Slips Option (replaced by the 310-9B Enhanced DS1 Testing Option)
- 310-9B Enhanced DS1 Testing Option
- 310-10 G.821 Results Option 310-10 G.821 Results Option
- 310-12 SONET OC-12 Transmit/Receive Option
- 310-13R SONET STS-1 Receive Option

- 310-13T SONET STS-1 Transmit Option
- 310-14R SONET STS-1, OC-1, OC-3 Receive Option (Replaces the 310-4A SONET Drop Option)
- 310-14T SONET STS-1, OC-1, OC-3 Transmit Option
- 310-15 OC-3c ATM Option
- 310-16 Optical Media Test Option

CONNECTIONS/
SETUPS

CONNECTIONS AND TEST SETUPS

2.1 T-BERD 310 CONNECTIONS

Figure 2-1 shows the location of the T-BERD 310 front-panel connections for transmitting and receiving DS3 signals. The DS3 TRANSMIT and DS3 RECEIVE jacks can connect the T-BERD 310 to a DS3 circuit at several DS3 access points. The access points can include the DS3 multiplexer, the DSX-3 patch panel, and the DS3 side of a long-haul transmission system.

Figure 2-2 identifies the typical access points where you can connect the T-BERD 310 for circuit and network testing. Table 2-1 lists the T-BERD 310 transmit and receive connection and level settings for the access points identified in Figure 2-2.

Along with the front-panel connections, the T-BERD 310 may have one or more of the side-panel connections shown in Figure 2-3. The side-panel connections enable the T-BERD 310 to transmit DS3 and DS1 signals; drop out DS1, E1, DS0, and VF signals to external test sets; analyze DS3 signals, DS1 signals, and SONET overhead from STS-1, OC-1, OC-3, OC-3c, and OC-12 signals; analyze both sides of a DS3 line; insert and test a DS1 channel in a live DS3 signal; and analyze the amplitude and frequency components of jitter. STS-1, OC-1, OC-3, OC-3c, and OC-12 signal inputs/outputs are also available to test SONET circuits.

The following side-panel connections are standard on the T-BERD 310 mainframe.

RS-232 interface connector — 25-pin D-type connector for printer or remote control operation.

MULTIPLE DS3 OUTPUT jacks — WECO 560A jacks (5 each) with the same output as the DS3 TRANSMIT jack.

DS1 DROP jack — Bantam jack that enables a DS1 signal to be dropped from either the primary DS3 receive input signal or a SONET option.

EXT CLOCK connector — BNC connector that enables an external input for a DS3 level clock source.

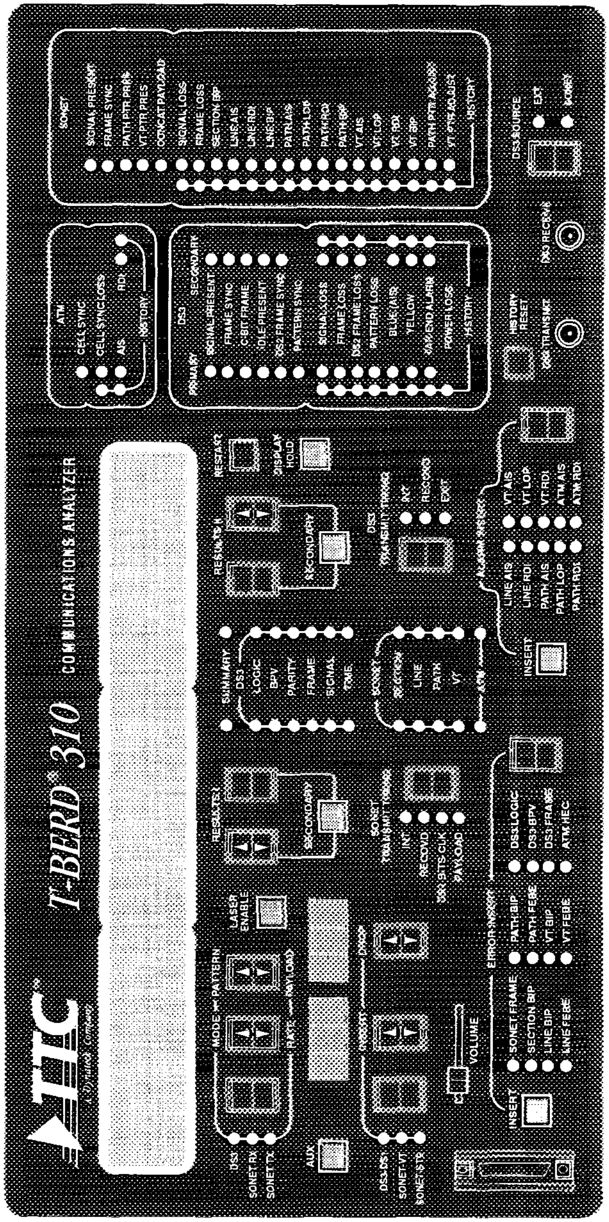

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Figure 2-1
T-BERD 310-S SONET/ATM Front Panel

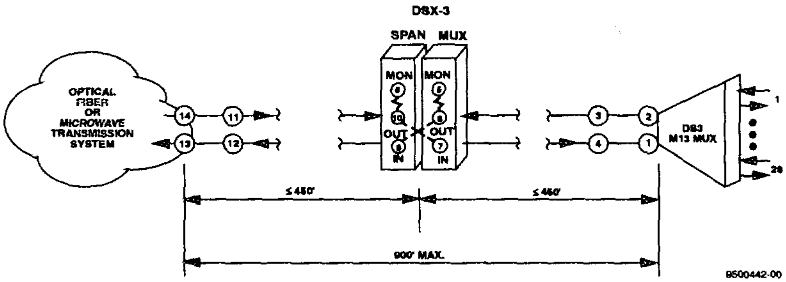


Figure 2-2
Typical DS3 Access Points

Table 2-1
T-BERD 310 DS3 Connections and Level Settings

Connections		Level Settings[1]		
TX	**RX**	**TX**	**RX**	**Description**
1	2	LOW[2]	HIGH	Connected across IN/OUT of multiplexer.
3	4	HIGH	LOW[2]	Connected across IN/OUT of cable, in place of the multiplexer.
—	5	—	DSX	Connected at MUX DSX-3 MON jack.
—	6	—	DSX	Connected at SPAN DSX-3 MON jack.
7	8	DSX	DSX	Connected across MUX DSX-3 IN/OUT jacks.
9	10	DSX	DSX	Connected across SPAN DSX-3 IN/OUT jacks.
11	12	HIGH	LOW[2]	Connected across IN/OUT of cable, in place of the transmission system.
13	14	LOW[2]	HIGH	Connected across IN/OUT of transmission system.

1 Set levels with MISC-DS3 LEVEL auxiliary function.

2 Use DSX if the cable length is less than 200 feet from the DSX-3 patch panel.

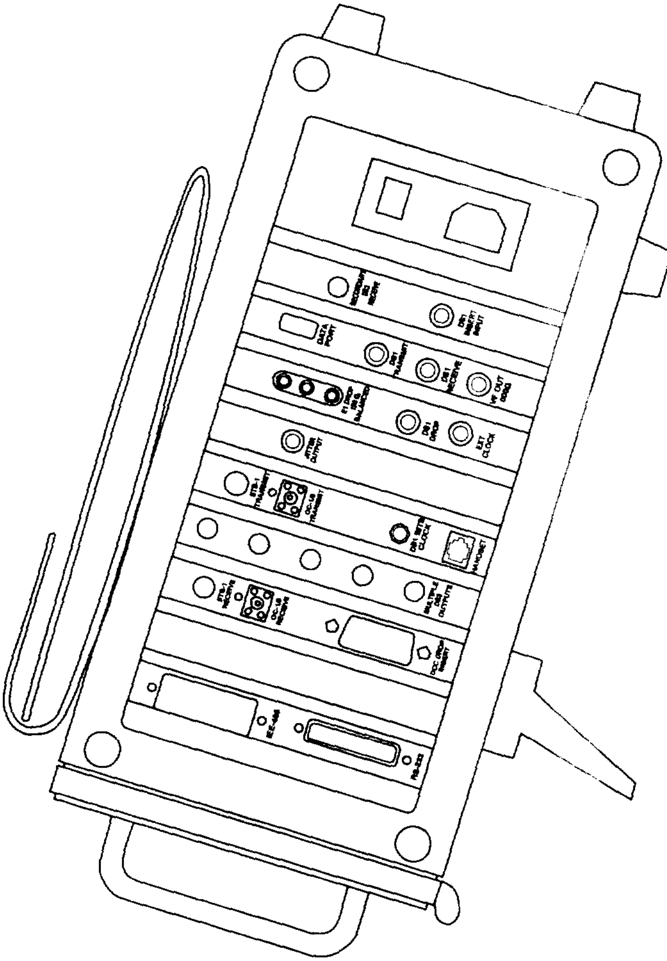


Figure 2-3
T-BERD 310 Side Panel Connections

The following side-panel connections are available on the indicated option.

310-1 DS1/DS0 Analyzer Option

VF OUT jack — Bantam jack with a 600 ohm terminated analog output.

DS1 TRANSMIT jack — Bantam jack with a DS1 output.

DS1 RECEIVE jack — Bantam jack for a DS1 input.

DATAPORT connector — 9-pin D-type connector that enables a DS0 channel or datalink (ESF, ESFz, or SLC) output.

310-2 E1 Drop Option

E1 DROP jack — 3-prong banana jack that enables an E1 signal to be dropped from either the primary DS3 receive input signal or a SONET DS3 payload.

310-3 DS1 Insert Option

DS1 INSERT INPUT jack — Bantam jack to insert a DS1 signal into a secondary DS3 signal.

SECONDARY DS3 RECEIVE jack — WECO 560A jack for a second DS3 input.

310-5 DS3 Jitter Option

JITTER OUTPUT jack — BNC jack with a demodulated output signal.

310-6 IEEE-488 Option

IEEE-488 interface connector — IEEE-488 connector for printer or remote control operation.

310-12 SONET OC-12 Transmit/Receive Option

OC-12 TRANSMIT connector — Selectable FC(PC) optical connector (ST® and SC connectors optional) for an OC-12 optical output.

OC-12 RECEIVE connector — Selectable FC(PC) optical connector for an OC-12 optical input.

LED illuminates when transmitting or receiving laser light.

310-13R SONET STS-1 Receive Option

STS-1 RECEIVE connector — WECO 560A connector for an STS-1 electrical input.

DCC DROP INSERT connector — RS-449 compatible, 15-pin, D-type, female connector for Line and Section DCC access.

310-13T SONET STS-1 Transmit Option

STS-1 TRANSMIT connector — WECO 560A connector for an STS-1 electrical output.

DS1 BITS CLOCK jack — Bantam jack for DS1 BITS clock input.

HANDSET jack — RJ-11 jack for orderwire channel handset.

310-14R SONET STS-1, OC-1, OC-3 Receive Option

STS-1 RECEIVE connector — WECO 560A connector for an STS-1 electrical input.

OC-1/OC-3 RECEIVE connector — Selectable FC(PC) optical connector (ST® and SC connectors optional) for an OC-1 or OC-3 optical input. LED illuminates when laser light is detected.

DCC DROP INSERT connector — RS-449 compatible, 15-pin, D-type female connector for Line and Section DCC access.

310-14T SONET STS-1, OC-1, OC-3 Transmit Option

STS-1 TRANSMIT connector — WECO 560A connector for an STS-1 electrical output.

OC-1/OC-3 TRANSMIT connector — Selectable FC(PC) optical connector (ST® and SC connectors optional) for an OC-1 or OC-3 optical output (LED illuminates when laser transmits light).

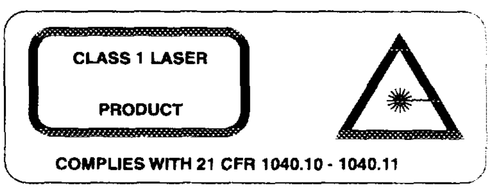
DS1 BITS CLOCK jack — Bantam jack for DS1 BITS clock input.

HANDSET jack — RJ-11 jack for orderwire channel handset.

310-16 Optical Media Test Option

POWER METER connector — FC(PC) connector allows an optical source to be connected to the T-BERD 310 to measure optical power.

RETURN LOSS/SOURCE connector — FC(UPC) optical connector (ST® and SC connectors optional) that allows return loss measurements to be performed or generate a stable optical output source. LED illuminates when laser transmits light.



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2.2 GENERATING PRINTOUTS

Use the following information to configure the T-BERD 310 and a compatible printer, such as the TTC PR-40A Thermal Printer, to generate results and controls printouts. You can connect either an RS-232 or IEEE-488 compatible printer to the T-BERD 310. The printer connections are found on the side panel.

Perform the following procedure to setup the T-BERD 310 to generate results and controls printouts. If a printer is not available, you can still generate printouts by storing them in the internal print buffer. The print buffer is maintained through power down. This procedure assumes you know how to setup the printer for proper operation (refer to the printer operating manual for operating procedures).

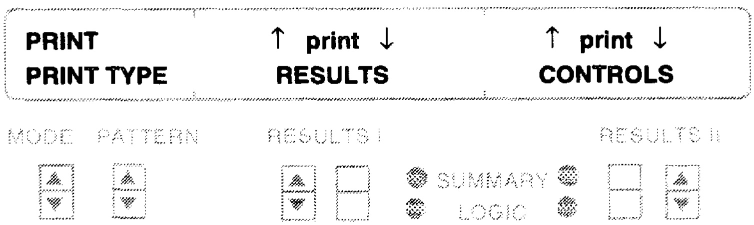
1. **Press the AUX switch (LED on) and set the following auxiliary functions:**

   Set the PRINT auxiliary group functions as follows:

Auxiliary Function	Selections	Comments
	Printout Control	
INTERVAL MODE	00:01 to 24:59, CONTINUOUS, or DELTA	Set the PRINT-PRINT EVENT auxiliary function to TIMED. Determines whether printed test results are accumulated throughout the test or are only accumulated between print events.
FORMAT	NORMAL, CUSTOM, or SUMMARY	Determines what results format is printed.
CUSTOM		Selects the results to be included in the custom results printout. Select the SUMMARY category to set the desired Status and Alarm LEDs and Far-End Alarm messages. Select the other categories to select the desired results.
WIDTH	40 or 80	Sets the printout line width
PRINT EVENT	OFF, 15 MIN, 30 MIN, TIMED, ERR SEC, or TEST END	Selects the print event for the results printout.
PRINT TYPE	RESULTS or CONTROLS	Generates the specified printout.
	RS-232 and IEEE-488 Interface Control	
BAUD RATE	110, 300, 600, 1200, 2400, 4800, or 9600	Sets the RS-232 interface baud rate.
PARITY	NONE, ODD, or EVEN	Sets the RS-232 interface parity. Set parity to NONE when printing pulse shape graphs.
TERMIN-ATOR	CR, LF, or CRLF	Sets printout line terminator. Set the terminator to CR when printing pulse shape graphs.
PORT	RS-232, IEEE-488, or IEEE-488 Talk-only	Selects printer interface port. This auxiliary function onlyappears when the 310-6 IEEE-488 Option is installed.

2. **Connect a printer to the T-BERD 310 (RS-232 or IEEE-488)**

3. **Select the PRINT-PRINT TYPE auxiliary function**
   Generate a results or controls printout to verify the proper operation of the printer and T-BERD 310. Press the **RESULTS I Results** switch to print a results printout and **RESULTS II Results** switch to print a controls printout.



4. **Press the AUX switch (LED off) to exit the auxiliary functions**

2.3 TIMED TEST SETUP

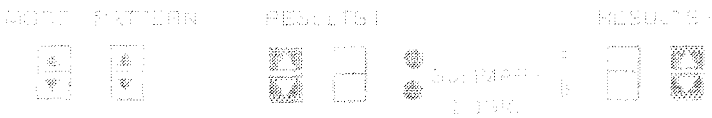
This procedure enables you to run an unattended test for an extended period and collect test results during and after the test. Perform the following procedure to setup the T-BERD 310 for a timed test and print the results at the end of the test. Specific results printouts are generated during the test by selecting the desired print event function with the PRINT-PRINT EVENT auxiliary function.

1. **Connect a compatible printer (optional)**
   Refer to Section 2.2 to connect a printer.

2. Press the AUX switch (LED on) and set the following auxiliary functions:

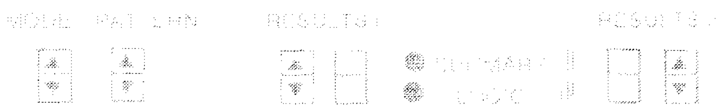
a. Select the TIME-TEST LENGTH auxiliary function to set the test length.

TIME	**↑ hour ↓**	**↑ minute ↓**
TEST LENGTH	**12**	**00**



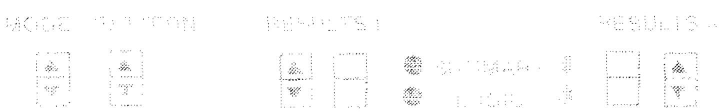
b. Select the PRINT-PRINT EVENT auxiliary function to set the print event to TEST END. The selection generates the test end results printout at the end of the test. The test end results printout can also be printed when the auxiliary function is set to TIMED.

PRINT	**↑ select ↓**
PRINT EVENT	**TEST END**



c. Select the TIME-TEST auxiliary function to set the test type to TIMED (changing from CONT to TIMED restarts the test).

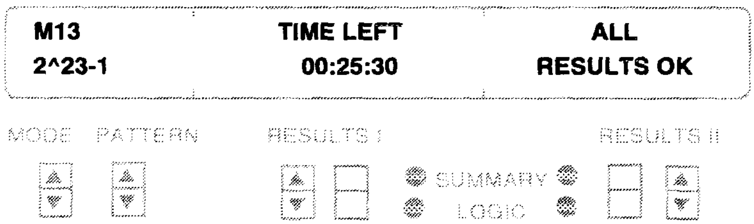
TIME	**↑ select ↓**
TEST	**TIMED**



3. **Press the AUX switch (LED off) to exit the auxiliary functions**

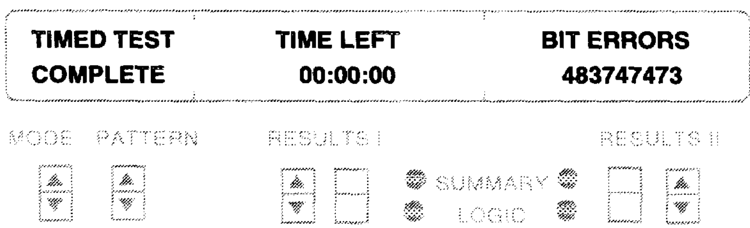
4. **Display timed test results**

   Select the TIME category TIME LEFT result in the RESULTS I window and the SUMMARY category in the RESULTS II window.



5. **T-BERD 310 displays completed timed test results**

   When the result equals 00:00:00, the test is complete, the message *TIMED TEST COMPLETE* flashes in the display, and the test result counts are frozen.



6. **Evaluate the test results**

   When the test is complete, evaluate the results by either scrolling through the frozen results or scanning the printouts.

DS3/DS1 MON.

DS3 MONITORING

T-BERD 310 Mainframe Setup

Results Interpretation

DS3/DS1 MONITORING

3.1 DS3 MONITORING

- Determine the performance of a live DS3 circuit in one direction without disrupting service.
- Monitor the DS3 signal for BPVs, frame errors, C-bit errors, parity errors, and Far-End Alarm messages.
- Measure the DS3 signal frequency.

Figure 3-1 illustrates how the T-BERD 310 connects to the DS3 circuit to analyze live data.

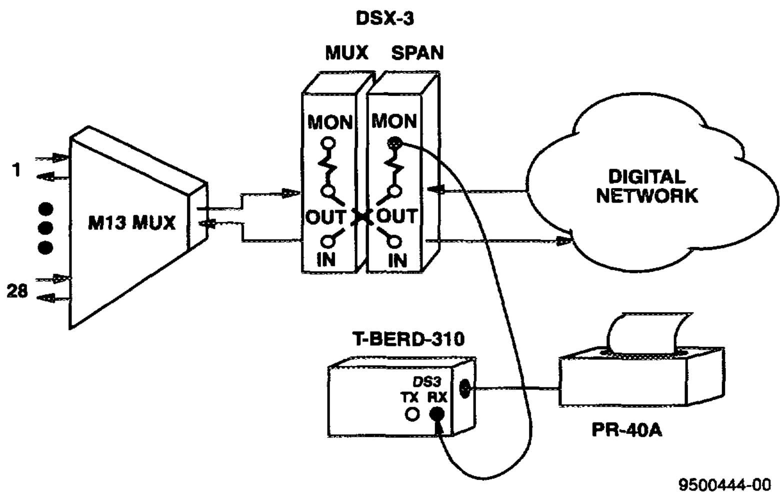


Figure 3-1
Monitoring DS3 Network Performance

3.1.1 T-BERD 310 Mainframe Setup

1. Connect a compatible printer (optional)

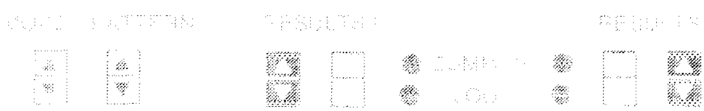
2. Set switches as follows:

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	AUTO
Channel Control	DS3-DS1

3. Press the AUX switch (LED on) and set the following auxiliary functions:

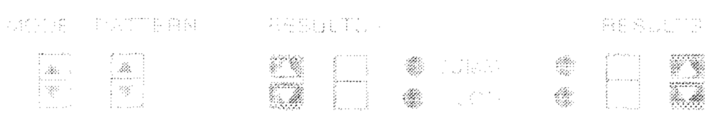
a. Select the MISC-BEEP CRI auxiliary function to select the beep criteria.

MISC	**↑ select ↓**	**↑ on off ↓**
BEEP CRI	**PATT SYNC**	**OFF**

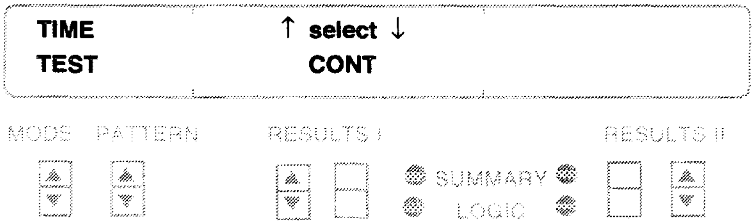


b. Select the MISC-DS3 LEVEL auxiliary function to select the DSX receive level.

MISC	**↑ transmit ↓**	**↑ receive ↓**
DS3 LEVEL	**DSX**	**DSX**



c. Select the TIME-TEST auxiliary function to select the test type.



4. Press the AUX switch (LED off) to exit the auxiliary functions

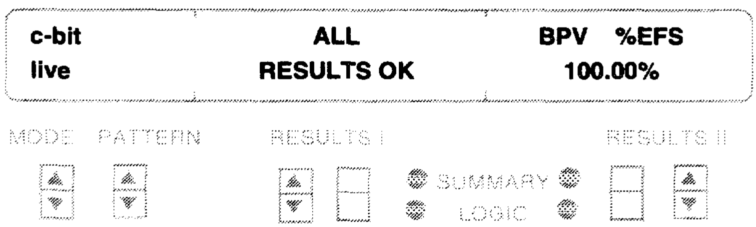
5. Set VOLUME switch to middle position

6. Connect the DS3 RECEIVE jack

Plug a cable between this jack and the span-side MONITOR jack.

7. Observe the MODE/PATTERN window

Verify the framing format and pattern.



8. Press the RESTART switch

Clear the old test results and start a new test.

9. Verify Primary DS3 Status LEDs

These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync (if applicable).

10. Verify RESULTS I test results

Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

3.1.2 Results Interpretation

When monitoring a DS3 line, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories.

BPV Category

BPV results — BPVs indicate problems with the local office equipment where the signal is being monitored. Since a BPV always causes a bit error, monitoring for BPVs provides an estimate of the number of bit errors occurring on an in-service line.

BPV THR ES — BPV threshold errored seconds indicate the number of errored seconds that exceed a specified error rate threshold. The threshold is set with the ERR RECEIVE-ERROR THR auxiliary function. This allows for exception reporting during long-term testing, counting severely errored seconds, or correlating error bursts with switchovers in protection switching.

PARITY Category

P-bit parity results (M13 and C-bit parity framing formats) — P-bit parity indicates the parity of the previously transmitted DS3 frame, and it is recalculated at each intermediate step in the transmission path by higher-order transmission systems. Therefore, P-bit parity results indicate signal integrity only on the last monitored leg of the transmission span.

C-bit parity results (C-bit parity framing format only) — C-bit parity is calculated only by terminating DS3 equipment at each end of the network, allowing C-bit parity results to indicate signal integrity from end to end.

Far-End Block Errors (FEBEs) results (C-bit parity framing format only) — If a C-bit parity or frame error is detected by the far-end equipment, the equipment detecting the error sends a FEBE back to the near end.

NOTE: Monitoring C-bit parity errors and FEBEs simultaneously allows both directions of the span to be evaluated from one location with one test set. If C-bit parity errors are being received, errors are being caused by the return leg of the DS3 span. If FEBEs are being received, errors are being caused on the transmitting leg of the DS3 span.

FRAME Category

Frame error results — Since the DS3 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS3 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.

FEOOF SEC — Far-End Out-Of-Frame Seconds indicate the DS3 equipment in the far-end direction has lost frame synchronization with the signal being transmitted from the near-end direction. This condition is also known as a Yellow Alarm or Remote Alarm Indication (RAI). A Yellow Alarm is transmitted by setting the X-bits to 00, and is applicable only with the C-bit parity framing format.

NEOOF SEC — Near-End Out-Of-Frame Seconds indicate the T-BERD 310 has lost frame synchronization with the received DS3 signal or has received a Blue Alarm (AIS). A near-end out-of-frame condition exists when excessive bit errors are occurring on the DS3 line, therefore corrupting the framing sequence.

DS2 FRM ERR — If the DS3 signal is channelized (the signal contains DS1, DS2, and DS3 framing bits), the DS2 and DS3 framing bits can be monitored for bit errors occurring in the DS3 payload. Monitoring DS2 frame errors also aids in isolating the cause of the errors between the DS3 and DS1 levels.

FRM THR ES — Frame threshold errored seconds indicate the number of errored seconds that exceed a specified error rate threshold. The threshold is set with the ERR RECEIVE-ERROR THR auxiliary function. This allows for exception reporting during long-term testing, counting severely errored seconds, or correlating error bursts with switchovers in protection switching.

SIGNAL Category

RX FREQ — An out-of-range frequency could indicate that a timing source is bad, or the timing source cannot recover the clock rate from the DS3 signal. The clock rate may not be recoverable if the DS3 signal does not maintain the 33% ones density rule, which could be caused by equipment improperly implementing B3ZS encoding. Also, since higher-order transmission equipment should not alter the DS3 frequency, an out-of-range frequency could be caused by DS3 transmission equipment such as a DS3 multiplexer.

Pulse shape results — The pulse shape can be monitored for changing trends in the signal performance. Refer to Section 6.1 to measure the pulse shape.

NOTE: Pulse Shape Results are only applicable at a DSX-3 out jack.

DS3 jitter results — Wideband and highband jitter can be monitored to isolate sources of DS3 jitter. Refer to Section 7 to measure the wideband and highband jitter.

BIDIRECTIONAL MONITORING

T-BERD 310 Mainframe Setup

Results Interpretation

3.2 BIDIRECTIONAL DS3 MONITORING

- Determine the performance of a live DS3 circuit in both directions without disrupting service.
- Monitor the DS3 signal for BPVs, frame errors, C-bit errors, parity errors, Far-End Block Errors, and Far-End Alarm messages on the primary and secondary sides of the DS3 circuit.
- Measure the DS3 signal frequency on the primary and secondary sides of the DS3 circuit.
- This application requires the 310-3 DS1 Insert Option.

Figure 3-2 illustrates the T-BERD 310 connection to the DS3 circuit to analyze live data on both sides of the line.

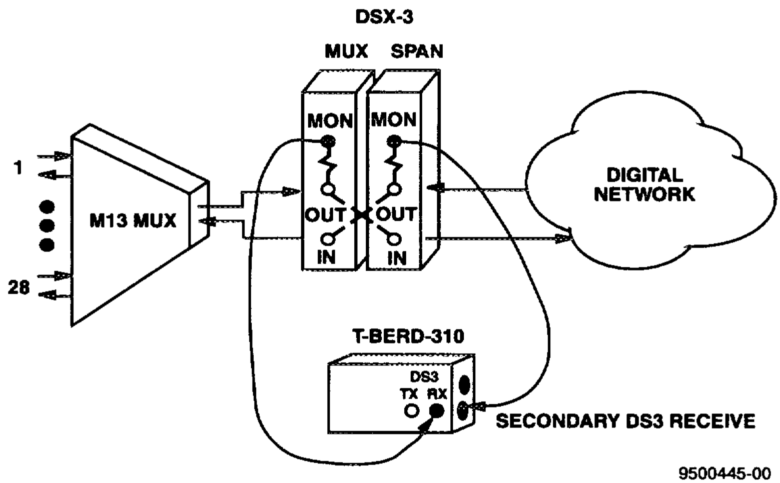


Figure 3-2
Monitoring Both Sides of a DS3 Line

3.2.1 T-BERD 310 Mainframe Setup

1. **Connect and monitor the primary DS3 signal**
   Perform the procedure in Section 3.1 to configure the T-BERD 310 for the primary side of the line.

2. **Connect the SECONDARY DS3 RECEIVE jack (side panel)**
   Plug a cable between this jack and the span-side MON jack.

3. **Press the RESTART switch**
   Clear the old test results and start a new test.

4. **Verify the Secondary DS3 Status LEDs**
   These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync (if applicable).

5. **Press the RESULTS II SECONDARY switch**
   The switch illuminates.

6. **Verify the secondary DS3 test results**
   Select the secondary SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

NOTE: The T-BERD 310 is equipped with an audible alarm that beeps when the error criteria are met. The audible alarm provides immediate notification the intermittent error has occurred. Set the beep criteria with the MISC-BEEP CRI auxiliary function.

3.2.2 Results Interpretation

Using dual DS3 receivers to monitor both sides simultaneously ensures the next error to occur is observed, minimizing test time. After looking at the error results for the primary and secondary DS3 receivers, the source direction that received the error can then be monitored using the primary DS3 receiver for complete in-service troubleshooting. When monitoring a DS3 line, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories.

Secondary Results

The C-BIT ERRORS, PAR ERRORS, FEBE, FRM ERRORS, VIOLATIONS, RX FREQ, and FEAC Code results that are used for performing in-service DS3 monitoring are also applicable to in-service bidirectional DS3 monitoring.

Primary Results

Once the source direction is known, the T-BERD 310 primary DS3 receiver can be used to troubleshoot the problem in the appropriate direction as described in Section 3.1.

DS1, E1, AND DS0 MONITORING FROM DS3 ACCESS POINTS

T-BERD 310 Mainframe Setup

310-1 DS1/DS0 Analyzer Option Setup

External DS1 Test Set Setup

310-2 E1 Drop Option Setup

310-1 Results Interpretation

3.3 DS1, E1, AND DS0 MONITORING FROM DS3 ACCESS POINTS

- Determine the performance of a live DS1 or E1 circuit from a DS3 access point without disrupting service.
- Monitor the DS1 signal for frame errors and CRC errors.
- Measure the DS1 signal frequency.
- Monitor DS0 channel signaling and VF level.
- Drop a DS0 channel to a speaker to determine voice quality.
- Drop an E1 channel to an E1 test set to analyze the E1 signal.
- Requires either the 310-1 DS1/DS0 Analyzer Option, an external DS1/DS0 test set (e.g., the T-BERD 211), or 310-2 E1 Drop Option and external E1 test set (e.g., the INTERCEPTOR 1402).

Figure 3-3 illustrates how the T-BERD 310 connects to the DS3 circuit to monitor and analyze the DS1/DS0 live data and drop an E1 channel.

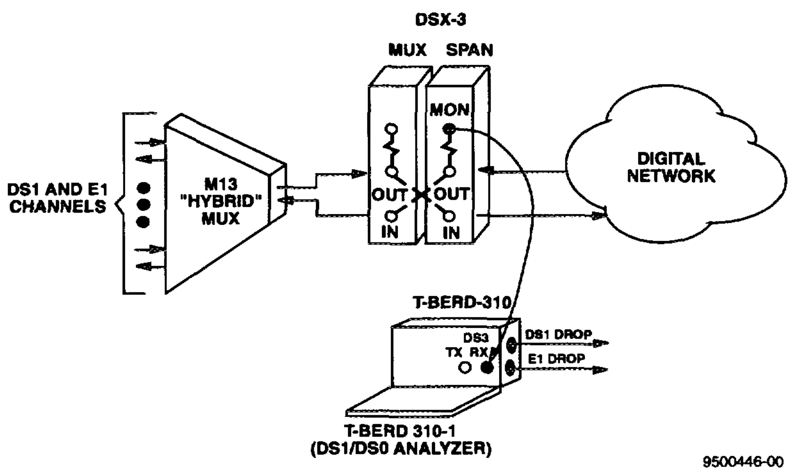


Figure 3-3
Monitoring DS1/DS0/E1 Channels from DSX-3 Patch Panel

3.3.1 T-BERD 310 Mainframe Setup

1. **Connect and monitor the DS3 signal**
   Perform the procedure in Section 3.1 to configure the T-BERD 310.

2. **Press the Channel Control switch and select DS3-DS1**

3. **Press the DROP switch**
   Select the desired DS1/E1 channel to be monitored.

   - To analyze the DS1 and DS0 channels, continue with the *310-1 DS1/DS0 Analyzer Option Setup* procedure. The DS1 channels appear as 1 to 28 in the DROP channel window.

   - To analyze the DS1 channels with an external DS1 test set, continue with the *External DS1 Test Set Setup* procedure. The DS1 channels appear as 1 to 28 in the DROP channel window.

   - If a SONET option is installed, select DS3 in the SONET RX-DS1 DROP OUT auxiliary function before selecting the DS1 channel.

   - To analyze the E1 channels, continue with the *310-2 E1 Drop Option Setup* procedure. The E1 channels appear as E1 to E21 in the DROP channel window.

3.3.2 310-1 DS1/DS0 Analyzer Option Setup

1. **Press the DS1 SOURCE switch**
   Select DS3 DROP (DS1 dropped from the T-BERD 310 mainframe).

2. **Press the MODE switch**
   Select AUTO.

3. Press the RESTART switch

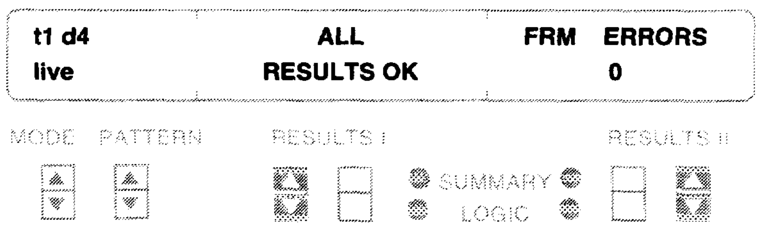
Clear the old test results and start a new test.

4. Verify the Status LEDs

These LEDs should illuminate: T1 Pulses and Frame Sync.

5. Observe the MODE/PATTERN window

Verify the framing format and pattern.



6. Verify the RESULTS I test results

Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

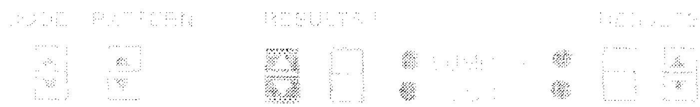
3.3.3 External DS1 Test Set Setup

1. Connect the T-BERD 310 DS1 DROP jack (side panel)

Connect the DS1 test set to this bantam or WECO 310 jack.

2. **Press the AUX switch (LED on) and set the following auxiliary functions(optional):**
   If a SONET receiver option is installed, set the SONET RX-DS1 DROP OUT auxiliary function to DS3. This drops the DS1 channel to the DS1 DROP jack from the DS3 signal.

SONET	**↑ select ↓**
DS1 DROP OUT	**DS3**



3. **Press the T-BERD 310 AUX switch (LED off) to exit the auxiliary functions**

4. **Verify the DS1 test results**
   Refer to the DS1 test set operating manual for signal analysis capabilities.

3.3.4 310-2 E1 Drop Option Setup

1. **Connect the T-BERD 310 E1 DROP jack (side panel)**
   Connect the E1 test set to this 3-prong banana jack.

2. **Verify the E1 test results**
   Refer to the E1 test set operating manual for signal analysis capabilities.

3.3.5 310-1 Results Interpretation

When monitoring a DS1 signal and DS0 channels from a DS3 access point, observe the results in the FRAME and SIGNAL categories.

NOTE: The BPV category and RX LVL dBdsx results are not applicable since the DS1 channel is dropped internally from within a DS3 signal.

FRAME Category

Frame error results — Since the DS1 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS1 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.

CRC error results (ESF framing only) — CRC errors indicate the integrity of the line at any error rate.

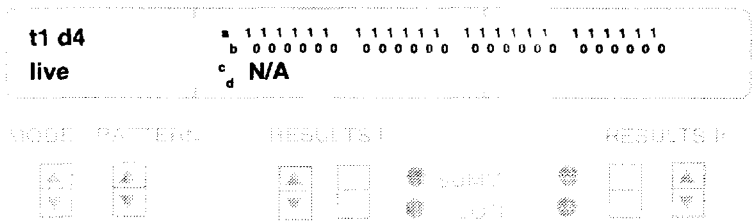
SIGNAL Category

The SIGNAL category results include both DS1 and DS0 measurements.

RX FREQ — The DS1 received frequency result is pertinent to DS1 signal processing. Note that if the received frequency is out of specification (< 1,543,923 or > 1,544,077 Hz) the result automatically appears in the SUMMARY category.

VF LVL dBm — The DS0 channel VF level can be measured while listening to the voice channel on the internal speaker.

abcd — The ABCD signaling bits are pertinent to DS0 channel signaling. The ABCD Signaling Bits result shows signaling bits for all 24 DS0s simultaneously, and provides an easy method to locate an active channel. The active channel can then be selected and listened to on the internal speaker.



DS1/DS0 MONITORING FROM DS1 ACCESS POINTS

310-1 DS1/DS0 Analyzer Option Setup

310-1 Results Interpretation

3.4 DS1/DS0 MONITORING FROM DS1 ACCESS POINTS

- Test DS1 channels without having to use another test set.
- Determine the performance of a live DS1 circuit from a DS1 access point without disrupting service.
- Monitor the DS1 signal for BPVs, frame errors, and CRC errors.
- Measure the DS1 signal frequency and DS1 level.
- Monitor DS0 channel signaling and VF level.
- This application requires the 310-1 DS1/DS0 Analyzer Option.

Figure 3-4 illustrates the T-BERD 310 connection to the DS1 circuit to monitor and analyze the DS1/DS0 live data.

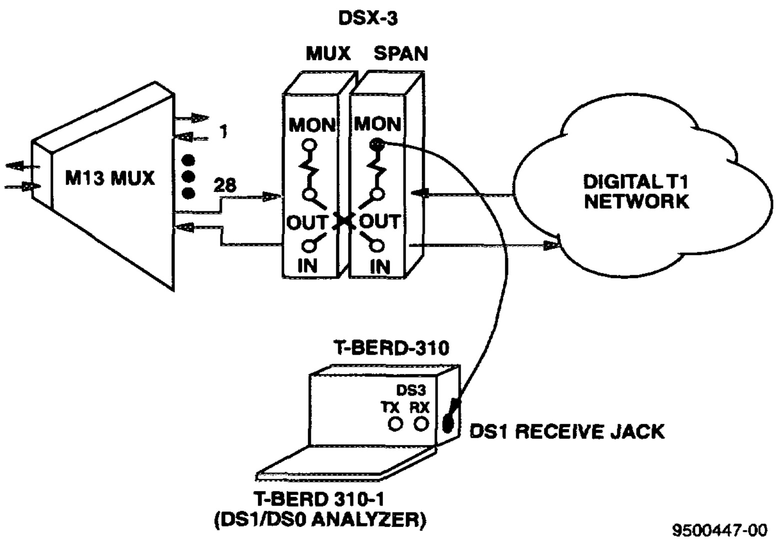


Figure 3-4
Monitoring DS1 Channels from the DSX-1 Patch Panel

310-1 DS1/DS0 Analyzer Option Setup

1. **Press the DS1 SOURCE switch**
   Select EXT. INPUT (side-panel DS1 RECEIVE jack).

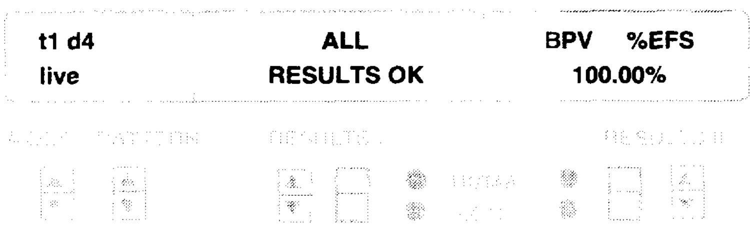
2. **Press the MODE switch**
   Select AUTO.

3. **Press the RECEIVE INPUT switch and connect the DS1 RECEIVE jack (side panel)**
   Select the DSX-MON input level and plug a cable between this jack and the span-side MON jack.

4. **Press the RESTART switch**
   Clear the old results and start a new test.

5. **Verify the Status LEDs**
   These LEDs should illuminate: T1 Pulses, Frame Sync, and B8ZS (if applicable).

6. **Observe the MODE/PATTERN window**
   Verify the framing format and pattern.



7. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

8. **Press the DS0 DROP CHANNEL switch**
   Select the desired DS0 channel.

9. **Set the T-BERD 310 VOLUME switch**
   Adjust to hear the DS0 channel.

310-1 Results Interpretation

When monitoring a DS1 signal and DS0 channels from a DS1 access point, observe the results in the BPV, FRAME, and SIGNAL categories.

BPV Category

BPV results — BPVs can be detected since the DS1 signal being analyzed is accessed directly from the DS1 access point. Since a BPV always causes a bit error, monitoring BPVs gives an estimate of the number of bit errors occurring on an in-service line.

FRAME Category

Frame error results — Since the DS1 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS1 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.

CRC error results (ESF framing only) — CRC errors indicate the integrity of the line at any error rate.

SIGNAL Category

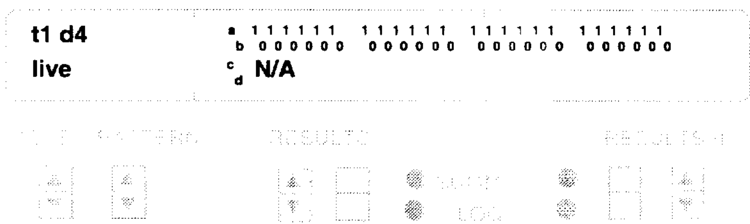
The SIGNAL category results include both DS1 and DS0 measurements.

RX LVL dBdsx — The DS1 receive level can be measured.

RX FREQ — The DS1 received frequency result is pertinent to DS1 signal processing. Note that if the received frequency is out of specification (< 1,543,923 or > 1,544,077 Hz) the result automatically appears in the SUMMARY category.

VF LVL dBm — The DS0 channel VF level can be measured while listening to the voice channel on the internal speaker.

abcd — The ABCD signaling bits are pertinent to DS0 channel signaling. The ABCD Signaling Bits result shows signaling bits for all 24 DS0s simultaneously, and provides an easy method to locate an active channel. The active channel can then be selected and listened to on the internal speaker.



DS1 TIMING SLIPS

3.5 DS1 TIMING SLIPS

- Measure timing slips relative to an external DS1 BITS Clock Source.
- Requires the 310-1, 310-9A/B, and 310-13T or 310-14T Options.

NOTE: Figure 3-5 shows the test access points and the T-BERD 310 reference sources, depending on the options installed. At a minimum, the 310-1 DS1/DS0 Analyzer Option and the 310-9A/B Option are necessary to perform timing slips measurements. Additional options are noted in parenthesis where the options increase flexibility to perform measurements.

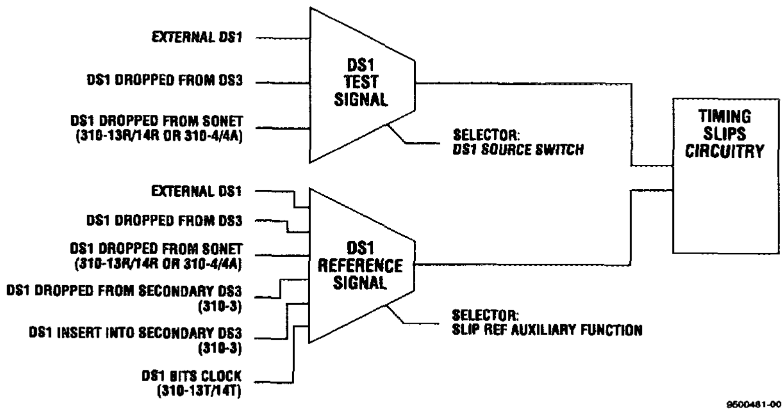


Figure 3-5
Possible DS1 Timing Slips Testing Configurations

3.5.1 Timing Slips Connections Setup

Figure 3-6 illustrates the text setup for measuring timing slips.

1. **Connect the reference signal**
   a. Press the 310-1 **AUX** switch and select the AUX-SLIP REF auxiliary function.
   b. Select the DS1 BITS CLOCK function.
   c. Connect a DS1 BITS clock source to the side-panel DS1 BITS CLOCK jack.

NOTE: Depending on the installed options, the AUX-SLIP REF auxiliary function can provide access for DS3, DS1, and SONET reference sources.

2. **Connect the test signal**
   Connect the test signal to the T-BERD 310 as follows:
   a. If the test signal is a DS1 embedded in SONET, follow the procedures in Section 3.5.2, *Test Setup for a DS1 Dropped from a SONET Source.*
   b. If the test signal is a DS1 embedded in DS3, follow the procedures in Section 3.5.3, *Test Setup for a DS1 Dropped from a DS3 Source.*
   c. If the test signal is an external DS1, follow the procedures in Section 3.5.4 *Test Setup for an External DS1 Source.*

3. **Set up the 310-1 DS1/DS0 Analyzer Option**
   Follow the procedures in Section 3.5.5 *310-1 DS1/DS0 Analyzer Option Setup* to prepare the T-BERD 310-1 DS1/DS0 Analyzer Option.

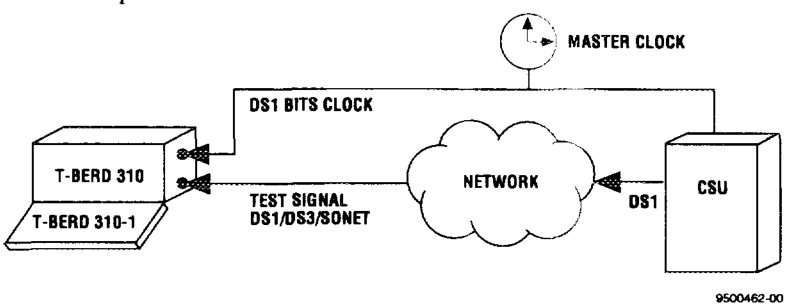


Figure 3-6
Possible DS1 Timing Slips Test Connections

3.5.2 Test Setup for DS1 Dropped from a SONET Source

1. **Connect the SONET signal source to a side panel connector: STS-1, OC-1, OC-3, or OC-12.**

2. **Select the SONET optical input rate:**
   a. Press the **Setup** switch to select SONET RX.
   b. Press the **RATE** switch to select the matching input rate.
   c. Press the **Channel Control** switch to select SONET-STS.
   d. Press the **DROP** switch to select the STS ID (1 to 3 for OC-3 or 1 to 12 for OC-12).

3. **Select the SONET automatic payload detection:**
   a. Press the **PAYLOAD** switch until AUTO appears.
   b. Press the **Channel Control** switch to select SONET-VT.
   c. Press the **DROP** switch to select the desired DS1 channel.

NOTE: Check to see that DS1 ASYNC or DS1 BYTE appears, indicating the proper payload. If it does not, check the test configuration. Also use Table 3-1 as a cross-reference to find the proper VT, since different mapping algorithms exist in SONET equipment.

4. **On the 310-1, set the DS1 SOURCE switch to SONET DROP**

5. **Proceed to Section 3.5.5, 310-1 DS1/DS0 Analyzer Option Setup**

3.5.3 Test Setup for DS1 Dropped from a DS3 Source

1. **Connect the DS3 signal to the DS3 RECEIVE jack**

2. **Set switches as follows:**

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	AUTO
Channel Control	DS3-DS1
DROP	select DS1 channel

Table 3-1
VT1.5 Translation

DS1 Channe Selection	M13 Group/ Channel	TR-253 Group/ Channel
1	1,1	1,1
2	1,2	2,1
3	1,3	3,1
4	1,4	4,1
5	2,1	5,1
6	2,2	6,1
7	2,3	7,1
8	2,4	1,2
9	3,1	2,2
10	3,2	3,2
11	3,3	4,2
12	3,4	5,2
13	4,1	6,2
14	4,2	7,2
15	4,3	1,3
16	4,4	2,3
17	5,1	3,3
18	5,2	4,3
19	5,3	5,3
20	5,4	6,3
21	6,1	7,3
21	6,2	1,4
23	6,3	2,4
24	6,4	3,4
25	7,1	4,4
27	7,2	5,4
27	7,3	6,4
28	7,4	7,4

3. **On the lid, set DS1 SOURCE switch to DS3 DROP**

4. **Proceed to Section 3.5.5, 310-1 DS1/DS0 Analyzer Option Setup**

3.5.4 Test Setup for an External DS1 Source

1. **Connect the DS1 signal to the side-panel DS1 RECEIVE jack**

2. **On the lid, set the DS1 SOURCE switch to EXT INPUT**

310-1 DS1/DS0 Analyzer Option Setup

1. **Press the RECEIVE INPUT switch to select TERM**

2. **Press the MODE switch to select AUTO**

3. **Verify the Status LEDs**
   Verify that only the following LEDs illuminate: T1 Pulses, Frame Sync, Pattern Sync, and B8ZS.

   NOTE: The B8ZS LED may not illuminate, depending on the line code; and the Pattern Sync LED does not illuminate for live traffic.

4. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected, verify the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Press the **RESULTS II Category** switch to select the SIGNAL category. Press the **RESULTS II Results** switch to examine the TIMING SLIPS result. Let the test run for at least 5 minutes, then check the result. If the result is non-zero, refer to *Timing Slips Results Interpretation* for additional information concerning the results.

3.5.6 Timing Slips Results Interpretation

SAME REF — The timing slips reference source selection is the same as the test source. Timing slips measurements would be invalid. Verify the setup of the AUX-SLIP REF auxiliary function setting and the **DS1 SOURCE** switch.

UNAVAILABLE — The DS1 signal selected by the **DS1 SOURCE** switch or the DS1 signal selected by the AUX-SLIP REF auxiliary function setting is either not connected or is not recoverable by the test set. Verify test configuration and connections.

CLK LOSS — The DS1 signal selected by the **DS1 SOURCE** switch has been disconnected. Verify test configuration and connections.

REF LOSS — The DS1 signal selected by the AUX-SLIP REF auxiliary function setting has been disconnected. Verify test configuration and connections.

NON-ZERO — The DS1 signal selected by the **DS1 SOURCE** switch is not properly synchronized to the DS1 signal selected by the AUX-SLIP REF auxiliary function.

DS3/DS1 BERT

DS3 LOOPBACK BERT TESTING AT DS3 ACCESS POINTS

T-BERD 310 Mainframe Setup

Results Interpretation

DS3/DS1 BERT TESTING

4.1 DS3 LOOPBACK BERT TESTING AT DS3 ACCESS POINTS

- Test the performance of a DS3 circuit from a DS3 access point during installation and acceptance testing.
- Loopback the DS3 signal at the far-end to verify circuit continuity.
- Test the DS3 circuit for logic errors, BPVs, frame errors, parity errors, and Far-End Alarm messages.
- Measure the DS3 signal frequency, level, and power.

Figure 4-1 illustrates the test setup with the T-BERD 310 at the near end and the loopback at the far end of the DS3 circuit.

4.1.1 T-BERD 310 Mainframe Setup

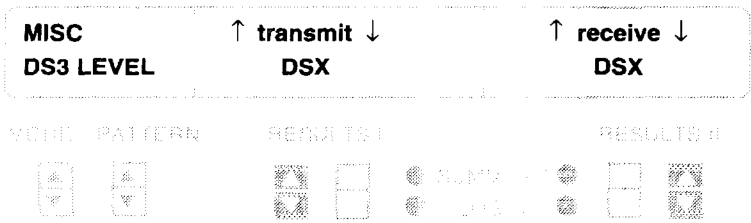
1. **Loopback the far end**
   Loopback the far end of the DS3 span at the DSX-3 patch panel.

2. **Set switches as follows:**

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	M13, C-BIT, or UNFRAMED
PATTERN	2^23-1
Channel Control	DS3-DS1
DS3 TRANSMIT TIMING	INT

3. Press the AUX switch (LED on) and set the following auxiliary functions:

Select the MISC-DS3 LEVEL auxiliary function to select the DSX receive level.



4. Press the AUX switch (LED off) to exit the auxiliary functions

5. Connect the DS3 RECEIVE jack

Plug a cable between this jack and the span-side OUT jack.

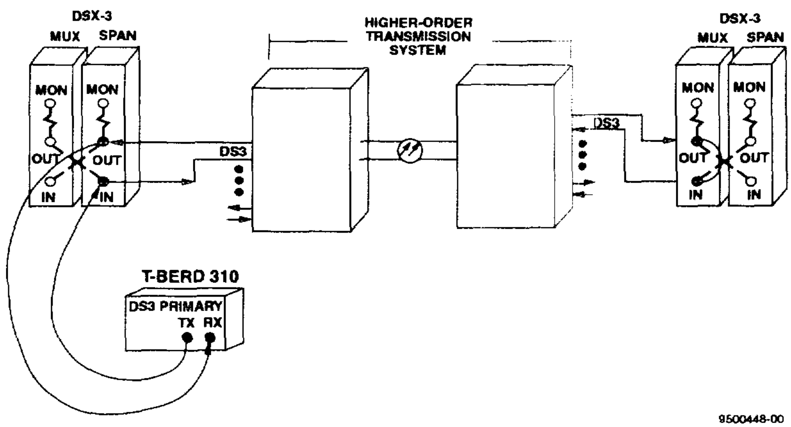


Figure 4-1
DS3 Loopback Testing

6. Connect the DS3 TRANSMIT jack

Plug a cable between this jack and the span-side IN jack.

7. Press the RESTART switch

Clear the old results and start a new test.

8. Verify Primary DS3 Status LEDs

These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and Pattern Sync.

9. Press the RESULTS I Category switch

Select the SUMMARY category.

10. Press the ERROR INSERT switch and select DS3 LOGIC

11. Press the INSERT switch

Press this switch quickly several times to send logic errors down the circuit. Verify the T-BERD 310 detects the errors and displays appropriate test results in the SUMMARY category. This verifies the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat this step.

12. Press the RESTART switch

Clear the old results and start a new test.

13. Verify the RESULTS I test results

Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

4.1.2 Results Interpretation

When performing an out-of-service DS3 bit error rate test, observe the results in the LOGIC, BPV, PARITY, FRAME, and SIGNAL categories.

LOGIC Category

Bit error results — DS3 bit error rate testing (BERT) involves transmitting a DS3 test pattern into the network, looping the signal back through the network, and comparing the transmitted and received signals bit by bit. Any change in the bit pattern is counted as a bit error. Verification the test pattern is received back through the network also ensures continuity along the entire transmission path. Since logic errors propagate through all transmission equipment, BERT can be used to test the end-to-end performance of a transmission system.

BIT THR ES — Bit threshold errored seconds indicate the number of errored seconds that exceed a specified error rate threshold. The threshold is set with the ERR RECEIVE-ERROR THR auxiliary function. This allows for exception reporting during long-term testing, counting severely errored seconds, or correlating error bursts with switchovers in protection switching.

BPV, PARITY, and FRAME Categories

If bit errors are occurring, the results used for in-service DS3 monitoring can also be used to isolate the error source. Refer to Section 3.1 for additional information.

SIGNAL Category

RX FREQ — An out-of-range frequency could indicate that a timing source is bad, or the timing source cannot recover the clock rate from the DS3 signal. The clock rate may not be recoverable if the DS3 signal does not maintain the 33% ones density rule, which could be caused by equipment improperly implementing B3ZS encoding. Also, since higher-order transmission equipment should not alter the DS3 frequency, an out-of-range frequency is probably caused by DS3 transmission equipment such as a DS3 multiplexer.

POWER — DS3 power measurements can be used to insure the network can supply and handle the maximum power requirements. Power measurements should be made using an unframed All Ones DS3 test pattern to insure maximum power usage. A framed All Ones pattern can be used, but the power reading will be up to 5% lower than the maximum power that could occur.

LEVEL — The signal level result indicates whether the transmission equipment is set to the proper line build-out (LBO). Improper LBO settings can cause the DS3 signal to be received either too weak or too strong for the receiving of equipment to handle.

Pulse shape results — The pulse shape can be measured and compared to industry pulse mask specifications. Refer to Section 6.2 to measure the pulse shape during a BERT test.

DS3 jitter results — Wideband and highband jitter can be monitored to isolate sources of DS3 jitter. Refer to Section 7 to measure the wideband and highband jitter.

Error Insertion

Logic, BPV, and frame error insertion can be used to test DS3 equipment recovery time, equipment tolerance, and alarm and protection switching. Use the **ERROR INSERT** switches and the ERR INSERT auxiliary group to insert controlled errors.

DS1 LOOPBACK BERT TESTING AT DS1 ACCESS POINTS

310-1 DS1/DS0 Analyzer Option Setup

310-1 Results Interpretation

4.2 DS1 LOOPBACK BERT TESTING AT DS1 ACCESS POINTS

- Test the performance of a DS1 circuit from a DS1 access point during installation and acceptance testing.
- Loopback the DS1 signal at a far-end CSU or NIU to verify circuit continuity.
- Test the DS1 circuit for logic errors, BPVs, frame errors, and CRC errors.
- Measure the DS1 signal frequency and level.
- Requires the 310-1 DS1/DS0 Analyzer Option and the 310-9B Enhanced DS1 Testing Option.

Figure 4-2 illustrates the test setup with the 310-1 DS1/DS0 Analyzer Option connected to the T1 circuit and the NIU is looped back.

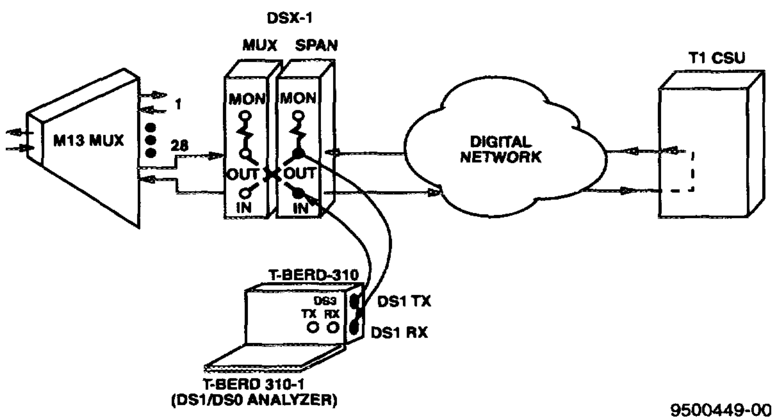


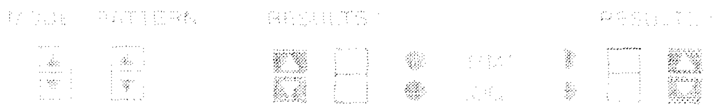
Figure 4-2
Testing a Looped Back DS1 Circuit

4.2.1 310-1 DS1/DS0 Analyzer Option Setup

1. **Press the AUX switch (LED on) and set the following auxiliary functions:**

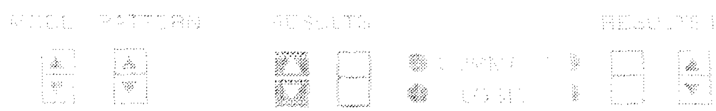
   a. Select the AUX-LP CODE auxiliary function to set the appropriate loop code. The in-band loop codes can be used in all framed modes. The ESF out-of-band loop codes can be used in the ESF mode.

AUX	**↑ in band ↓**	**↑ out of band ↓**
LP CODE	**FAC1**	**LINE**



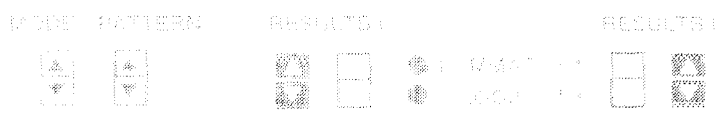
   b. Select the AUX-ESF LOOP auxiliary function to set the ESF loop code type.

AUX	**↑ select ↓**
ESF LOOP	**IN BAND**



   c. Select the AUX-PRM auxiliary function to set the ESF PRM transmit and receive functions.

AUX	**↑ prm transmit ↓**	**↑ prm rcvr ↓**
PRM	**OFF**	**ON**



2. **Press the AUX switch (LED off)**
   Exit the auxiliary functions.

3. **Set switches as follows:**

DS1 SOURCE	EXT. INPUT (side-panel DS1 RECEIVE jack).
MODE	T1 D4, T1 ESF, or T1
PATTERN	QRSS (ALL ZEROS can be used to detect improper line coding)
TRANSMIT TIMING	INTERNAL
CODE	AMI or B8ZS
RECEIVE INPUT	TERM

4. **Connect the DS1 RECEIVE jack (side panel)**
   Plug a cable between this jack and the span-side OUT jack.

5. **Connect the DS1 TRANSMIT jack (side panel)**
   Plug a cable between this jack and the span-side IN jack.

6. **Press the LOOP UP switch**
   Transmit the selected loop-up code. When the loopback is accomplished, the switch LED goes off and the loop code message is replaced with the selected test pattern.

7. **Press the RESULTS I Category switch**
   Select the SUMMARY category.

8. **Press the LOGIC ERROR INSERT switch**
   Press this switch quickly several times to send logic errors down the circuit. Verify the 310-1 detects the errors and displays appropriate test results in the SUMMARY category. This verifies the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat the step.

9. **Press the RESTART switch**
   Clear the old results and start a new test.

10. **Verify the Status LEDs**
    These LEDs should illuminate: T1 Pulses, Frame Sync, Pattern Sync, and B8ZS (if applicable).

11. **Verify the RESULTS I test results**
    Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

4.2.2 310-1 Results Interpretation

When performing an out-of-service DS1 bit error rate test, observe the results in the LOGIC, BPV, FRAME, and SIGNAL categories on the lid.

SUMMARY Category

B8ZS Detected — Indicates the received line coding is B8ZS even though the transmitted line code from the 310-1 is AMI.

LOGIC Category

Bit error results — DS1 bit error rate testing (BERT) involves transmitting a DS1 test pattern into the network, looping the signal back through the network, and comparing the transmitted and received signals bit by bit. Any change in the bit pattern is counted as a bit error. Verification the test pattern is received back through the network also insures continuity along the entire transmission path. Since logic errors propagate through all transmission equipment, BERT testing can be used to test the end-to-end performance of a transmission system.

BIT THR ES — Bit threshold errored seconds indicate the number of errored seconds that exceed a specified error rate threshold. The threshold is set with the ERR RECEIVE-ERROR THR auxiliary function. This allows for exception reporting during long-term testing, counting severely errored seconds, or correlating error bursts with switchovers in protection switching.

BPV, FRAME, and SIGNAL Categories

If bit errors are occurring, the results used for in-service DS1 monitoring can also be used to isolate the error source. Refer to Section 3.4 for additional information.

INSERT DS1
IN DS3

INSERTING DS1 SIGNALS INTO LIVE DS3 SIGNALS

5.1 DS1 INSERT OPTION SIGNAL FLOW

The 310-3 DS1 Insert Option allows the T-BERD 310 to insert a DS1 channel into a live multiplexed DS3 signal. The option also equips the T-BERD 310 with a secondary DS3 receiver as described in Section 3.2, *Bidirectional DS3 Monitoring.*

Figure 5-1 illustrates the signal flow when performing DS1 drop and insert testing. A DS1 signal is inserted into a selected channel of the secondary DS3 receive input. The DS1 signal can be sourced internally from the 310-1 DS1/DS0 Analyzer Option, or externally from the DS1 INSERT input. The DS1 channel can then be looped back into the returning DS3 signal. This DS3 signal is then accepted by the primary DS3 receive input for analysis. The DS1 channel can then be dropped and analyzed by either the 310-1 DS1/DS0 Analyzer Option or by an external DS1 test set.

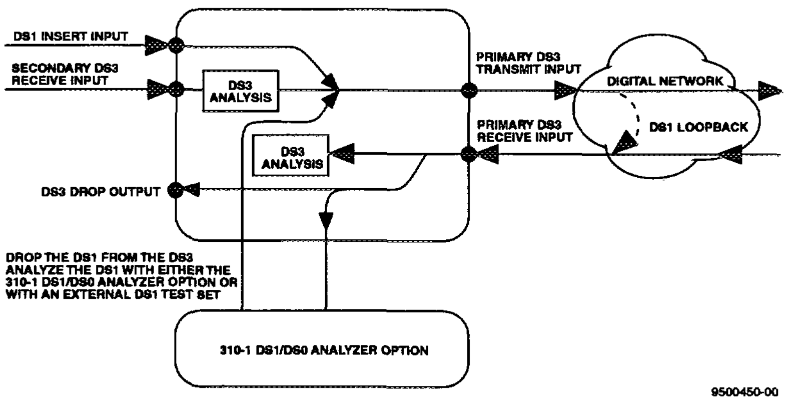


Figure 5-1
DS1 Insert Option Signal Flow Diagram

INSERTING AN INTERNAL DS1 SIGNAL INTO A LIVE DS3 SIGNAL

5.2 INSERTING AN INTERNAL DS1 SIGNAL INTO A LIVE DS3 SIGNAL

- Access a live DS3 signal and drop and insert a DS1 signal from an internal source.
- Perform an out-of-service loopback test on a DS1 channel of a live DS3 signal.
- Insert an internally generated DS1 test pattern or loop code.
- Perform a bit error rate test on the out-of-service DS1 channel.
- Requires the 310-3 DS1 Insert Option and the 310-1 DS1/DS0 Analyzer Option.
- Requires a 75 ohm terminator.

NOTE: When this procedure is performed properly, the DS3 signal is momentarily disrupted and only the selected DS1 channel is placed out of service.

Figure 5-2 shows the T-BERD 310 connected to the DSX-3 patch panel. The 310-1 DS1/DS0 Analyzer Option provides the inserted DS1 channel test pattern and DS1 analysis capabilities.

5.2.1 T-BERD 310 Mainframe Setup, Part 1

1. Set switches as follows:

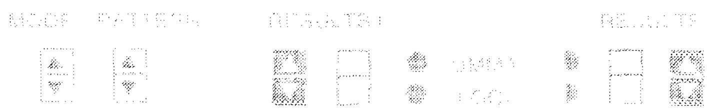
DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	DS1 INSERT
PATTERN	INTERNAL DS1 (pattern from 310-1 Option).
Channel Control	DS3-DS1

NOTE: When selecting the DS1 INSERT mode, transmit timing defaults to recovered and "— — —" appears in the INSERT window indicating that no DS1 signal is being inserted at this time (i.e., all DS1s in the signal are passed through the test set back into the span). The **INSERT** switch should remain in this position until the 310-1 DS1/DS0 Analyzer Option is configured.

2. **Press the AUX switch (LED on) and set the following auxiliary functions:**

   Select the MISC-DS3 LEVEL auxiliary function to select the DSX receive level.

MISC	↑ **transmit** ↓	↑ **receive** ↓
DS3 LEVEL	**DSX**	**DSX**



3. **Press the AUX switch (LED off) to exit the auxiliary functions**

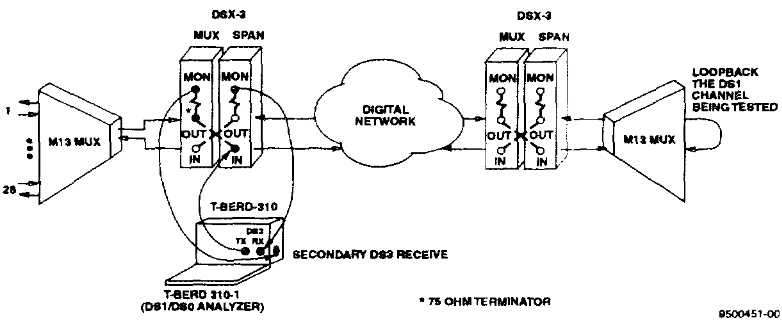


Figure 5-2
Inserting an Internally Generated DS1 Signal into a Live DS3 Signal

4. **Connect the SECONDARY DS3 RECEIVE jack (side panel)**
   Plug a cable between this jack and the multiplexer-side MON jack. The T-BERD 310 automatically configures itself to the received signal.

5. **Press the RESTART switch**
   Clear the old results and start a new test.

6. **Verify the Secondary DS3 Status LEDs**
   These LEDs should illuminate: Signal Present, Frame Sync, DS2 Frame Sync, and C-Bit Frame (if applicable).

   NOTE: If the secondary DS3 signal is not detected (Secondary Signal Present and Secondary Frame Sync LEDs are not illuminated), do not proceed with the next step until the signal and framing are detected.

7. **Connect the DS3 TRANSMIT jack**
   Plug a cable between this jack and the span-side IN jack. This should only produce a brief interruption to the DS3 line. Plug the cable into the T-BERD 310 first, then the patch panel to minimize the interruption.

8. **Plug in the 75 ohm terminator into the multiplexer-side OUT jack**

9. **Connect the DS3 RECEIVE jack**
   Plug a cable between this jack and the span-side MONITOR jack.

10. **Press the RESTART switch**
    Clear the old results and start a new test.

11. **Verify the Primary DS3 Status LEDs**
    These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync.

12. **Verify the RESULTS I and II test results**

    Select the primary SUMMARY category in the RESULTS I window. Select the secondary SUMMARY category in the RESULTS II window by pressing the **SECONDARY** switch until the LED is illuminated. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

5.2.2 310-1 DS1/DS0 Analyzer Option Setup, Part 1

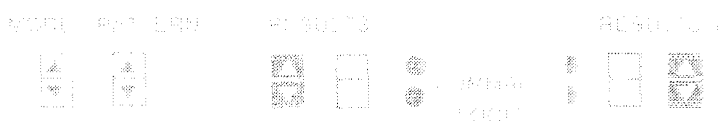
13. **Set switches as follows:**

DS1 SOURCE	DS3 DROP (DS1 dropped from T-BERD 310).
MODE	T1 D4, T1 ESF, or T1
PATTERN	QRSS
TRANSMIT TIMING	INTERNAL

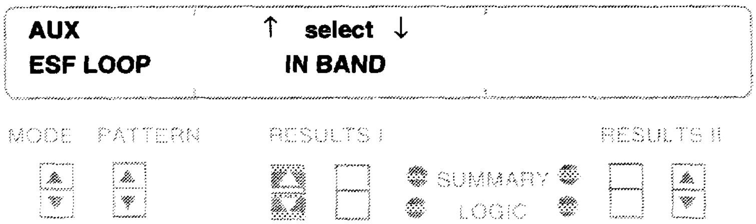
14. **Press the AUX switch (LED on) and set the following auxiliary functions:**

    a. Select the AUX-LP CODE auxiliary function to set the appropriate loop code. The in-band loop codes can be used in all framed modes. The ESF out-of-band loop codes can be used in the ESF mode.

AUX	**↑ in band ↓**	**↑ out of band ↓**
LP CODE	**CSU**	**LINE**



b. Select the AUX-ESF LOOP auxiliary function to set the ESF loop code type.



15. Press the AUX switch (LED off)

Exit the auxiliary functions.

5.2.3 T-BERD 310 Mainframe Setup, Part 2

16. Press the Channel Control switch and select DS3-DS1

17. Press the DROP switch

Select the desired DS1 channel to be dropped.

18. Press the INSERT switch

Select the desired DS1 channel of the secondary DS3 received signal that is going to accept the DS1 signal from the 310-1 DS1/DS0 Analyzer Option. The selected channel number flashes several times in the window, allowing the user to change the channel selection without disrupting T1 service. When the channel number stops flashing, the DS1 channel is out-of-service; the other 27 channels are not affected.

5.2.4 310-1 DS1/DS0 Analyzer Option Setup, Part 2

19. Press the LOOP UP switch

Transmit the selected loop-up code. When the loopback is accomplished, the switch LED goes off and the loop code message is replaced with the selected test pattern.

20. Verify the Status LEDs

These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

21. Press the LOGIC ERROR INSERT switch

Press this switch several times to send logic errors down the circuit. Verify the 310-1 detects the errors and displays appropriate test results in the SUMMARY category. This verifies the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat this step.

22. Press the RESTART switch

Clear the old results and start a new test.

23. Verify the RESULTS I test results

Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

24. Press the LOOP DOWN switch

Transmit the selected loop-down code. When the loopback is released, the switch LED goes off and the loop code message is replaced with the selected test pattern.

25. Repeat Steps 16 to 24 for the next DS1 channel

5.2.5 Disconnecting the T-BERD 310, Part 3

NOTE: Perform the following steps in the indicated order to minimize a disruption of the DS3 signal.

26. Press the 310-1 LOOP DOWN switch
Transmit the selected loop-down code to release the far-end loopback.

27. Press the INSERT switch
Display the "— — —" in the INSERT window.

28. Unplug the cable from the span-side MONITOR jack (see Figure 5-2)

29. Unplug the 75 ohm terminator from the multiplexer-side OUT jack

30. Unplug the cable from the span-side IN jack

31. Unplug the cable from the multiplexer-side MONITOR jack

5.2.6 T-BERD 310 Results Interpretation

Using the dual DS3 receivers enables T-BERD 310 to verify the DS3 signal quality in both directions before inserting the DS1 channel. Refer to Section 3.2, *Results Interpretation*, to verify the DS3 signal is error free. When monitoring a DS3 line, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories.

5.2.7 310-1 Results Interpretation

The insertion of a DS1 test pattern into a live DS3 signal is a means of allowing complete out-of-service DS1 testing from a DS3 access point. Except for the BPV category and the RX LVL dBdsx result (since the DS1 channel is internally dropped from the DS3 signal), the results for out-of-service DS1 BERT testing (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when performing DS1 insert testing.

INSERTING AN EXTERNAL DS1 SIGNAL INTO A LIVE DS3 SIGNAL

5.3 INSERTING AN EXTERNAL DS1 SIGNAL INTO A LIVE DS3 SIGNAL

- Access a live DS3 signal and drop and insert a DS1 signal from an external DS1 source (e.g., T-BERD 211).
- Perform an out-of-service loopback test on a DS1 channel of a live DS3 signal.
- Insert an externally generated DS1 test pattern or loop code.
- Perform a bit error rate test on the out-of-service DS1 channel.
- Requires the 310-3 DS1 Insert Option.
- Requires a 75 ohm terminator.

NOTE: When this procedure is performed properly, the DS3 signal is unaffected and only one DS1 channel is placed out of service.

Figure 5-3 shows the T-BERD 310 connected to the DSX-3 patch panel. The external DS1 source provides the inserted DS1 channel test pattern and DS1 analysis capabilities.

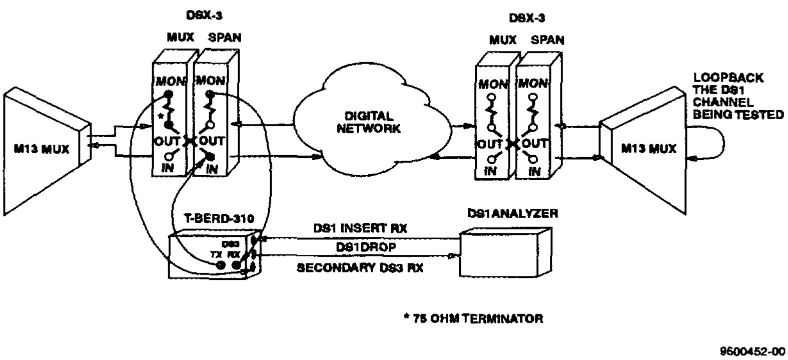


Figure 5-3
Inserting an Externally Generated DS1 Signal into a Live DS3 Signal

5.3.1 T-BERD 310 Mainframe Setup, Part 1

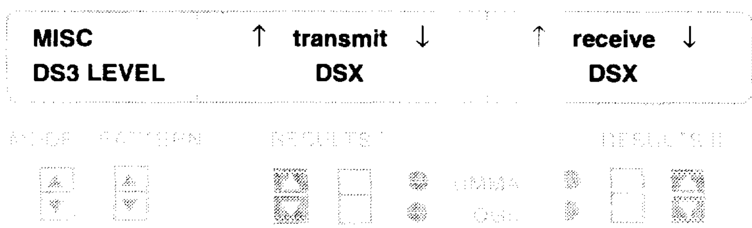
1. Set switches as follows:

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	DS1 INSERT
PATTERN	EXTERNAL DS1 (pattern from DS1 INSERT INPUT jack).
Channel Control	DS3-DS1

NOTE: When selecting the DS1 INSERT mode, transmit timing defaults to recovered and "— — —" appears in the INSERT window indicating that no DS1 signal is being inserted at this time (i.e., all DS1s in the signal are passed through the test set back into the span). The **INSERT** switch should remain in this position until the external DS1 signal source is configured.

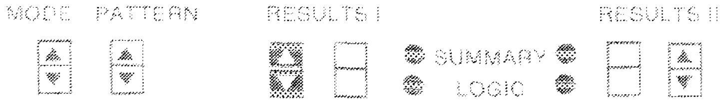
2. Press the AUX switch (LED on) and set the following auxiliary functions:

a. Select the MISC-DS3 LEVEL auxiliary function to select the DSX receive level.



b. Select the MISC-DS1 LINECODE auxiliary function to set the transmitted line coding for the DS1 DROP jack (side panel) signal.

MISC	↑ select ↓	
DS1 LINECODE	AMI	



3. Press the AUX switch (LED off) to exit the auxiliary functions

4. Connect the SECONDARY DS3 RECEIVE jack (side panel)

Plug a cable between this jack and the multiplexer-side MON jack. The T-BERD 310 automatically configures itself to the received signal.

5. Press the RESTART switch

Clear the old results and start a new test.

6. Verify the Secondary DS3 Status LEDs

These LEDs should illuminate: Signal Present, Frame Sync, and C-Bit Frame (if applicable).

NOTE: If the secondary DS3 signal is not detected (Secondary Signal Present and Secondary Frame Sync LEDs are not illuminated), do not proceed with the next step until the signal and framing are detected.

7. Connect the DS3 TRANSMIT jack

Plug a cable between this jack and the span-side IN jack. This should only produce a brief interruption to the DS3 line. Plug the cable into the T-BERD 310 first, then the patch panel to prevent lengthy interruptions.

8. Plug in the 75 ohm terminator into the multiplexer-side OUT jack

9. Connect the DS3 RECEIVE jack
Select the DSX input level and plug a cable between this jack and the span-side MONITOR jack.

10. Press the RESTART switch
Clear the old results and start a new test.

11. Verify the Primary DS3 Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync.

12. Verify the RESULTS I and II test results
Select the primary SUMMARY category in the RESULTS I window. Select the secondary SUMMARY category in the RESULTS II window. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

5.3.2 External DS1 Test Set Setup, Part 1

13. Set the operating mode
Select an appropriately framed DS1 operating mode, e.g., D4, ESF, SLC-96, or FT1.

14. Set the test pattern
Select an appropriate DS1 test pattern, e.g., QRSS.

15. Set the transmit timing
Select INTERNAL.

16. Set the receive input termination and connection
Select the TERM input level and connect the DS1 test set receive input connection to the T-BERD 310 DS1 DROP jack (side panel).

17. Set the transmit output termination and connection

Select the 0dB (DSX) output level and connect the DS1 test set transmit output connection to the T-BERD 310 DS1 INSERT INPUT jack (side panel).

18. Configure the loop code function

If the DS1 test set has the capability of transmitting and receiving loop codes, configure the test set to transmit and receive the appropriate loop codes.

19. Verify the DS1 test results

Display the appropriate test results.

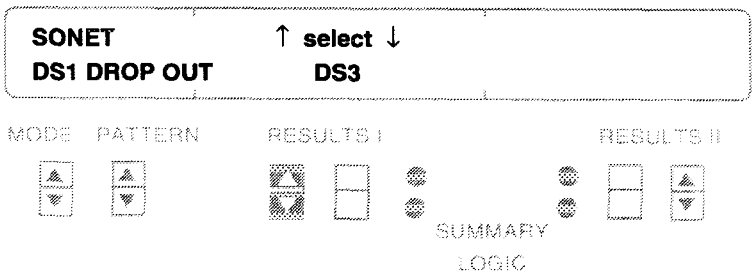
5.3.3 T-BERD 310 Mainframe Setup, Part 2

20. Press the DROP switch

Select the desired DS1 channel to be dropped through the DS1 DROP jack (side panel) and to the external DS1 test set.

21. Press the AUX/MODE/PATTERN switches (optional)

If a SONET receiver option is installed, set the SONET RX-DS1 DROP OUT auxiliary function to DS3. This drops the DS1 channel from the DS3 signal to the DS1 DROP jack (side panel).



22. Press the AUX switch (LED off)

Exit the auxiliary functions.

23. Press the INSERT switch

Select the desired DS1 channel of the secondary DS3 received signal that is going to accept the DS1 signal from the DS1 test set. As long as the channel number is flashing in the window, the channel can be changed without affecting the DS1 channel. When the channel number stops flashing the DS1 channel is out-of-service; the other 27 channels are not affected.

5.3.4 External DS1 Test Set Setup, Part 2

24. Establish a DS1 channel loopback

Establish a DS1 channel loopback at the far end of the circuit.

25. Verify the received signal status

Determine if the external DS1 test set has acquired the received DS1 signal.

26. Verify the received signal alarm status

Determine if the external DS1 test set has detected any alarmed conditions.

27. Insert logic errors

Send logic errors down the circuit and verify the DS1 test set is receiving the proper DS1 signal and errors. This verifies the transmitted signal is being looped back and received.

28. Restart the DS1 test set

Clear the old results and start a new test.

29. Verify the DS1 test results

Refer to *External Test Set Results Interpretation* for additional information concerning the results.

30. Release the DS1 channel loopback

Release the DS1 channel loopback at the far end of the circuit.

31. Repeat Steps 20 to 30 for the next DS1 channel

5.3.5 Disconnecting the T-BERD 310, Part 3

NOTE: Perform the following steps in the indicated order to prevent a disruption of the DS3 signal.

32. Release the DS1 channel loopback
Release the DS1 channel loopback at the far end of the circuit.

33. Press the INSERT switch
Display the "— — —" in the INSERT window.

34. Unplug the cable from the span-side MONITOR jack (see Figure 5-3)

35. Unplug the 75 ohm terminator from the multiplexer-side OUT jack

36. Unplug the cable from the span-side IN jack

37. Unplug the cable from the multiplexer-side MONITOR jack

5.3.6 T-BERD 310 Results Interpretation

Using the dual DS3 receivers enables T-BERD 310 to verify the DS3 signal quality in both directions before inserting the DS1 channel. Refer to Section 3.2, *Results Interpretation*, to verify the DS3 signal is error free. When monitoring a DS3 line, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories.

5.3.7 External Test Set Results Interpretation

The insertion of a DS1 test pattern into a live DS3 signal is a means of allowing complete out-of-service DS1 testing from a DS3 access point. Except for BPV results and the receive level result, the results for out-of-service DS1 BERT testing and in-service DS1 monitoring are also applicable when performing DS1 insert testing. Refer to the DS1 test set operating manual for signal analysis capabilities. Full bit error rate testing can be performed on the selected DS1 channel.

DS3 PULSE
SHAPE

IN-SERVICE DS3 SIGNAL ANALYSIS

T-BERD 310 Mainframe Setup

Results Interpretation

DS3 PULSE SHAPE ANALYSIS

6.1 IN-SERVICE DS3 SIGNAL ANALYSIS

- Monitor the DS3 pulse width, rise time, and fall time on a live circuit.
- Perform DS3 pulse shape analysis at any time while monitoring a live circuit.
- DS3 pulse width, rise time, and fall time can be measured from the DSX-3 MONITOR jack to establish a benchmark of the signal quality while monitoring a live circuit.
- Generate a pulse shape graph showing the pulse shape, width, rise time, and fall time for permanent records.

6.1.1 T-BERD 310 MAINFRAME SETUP

1. **Set switches as follows:**

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	AUTO

NOTE: The DS3 pulse shape analysis can only be performed from the DS3 RECEIVE jack.

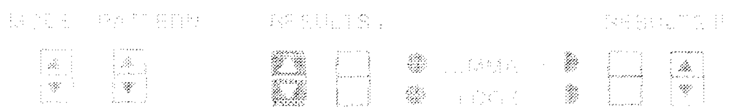
2. **Press the AUX switch (LED on) and set the following auxiliary functions:**

   a. Select the MISC-DS3 LEVEL auxiliary function to select the DSX receive level.

MISC	↑ **transmit** ↓	↑ **receive** ↓
DS3 LEVEL	**DSX**	**DSX**

   b. Select the MISC-PULSE MASK auxiliary function and set to NONE.

MISC	↑ **select** ↓
PULSE MASK	**NONE**



NOTE: The PULSE SHAPE result only applies when the MISC-PULSE MASK auxiliary function is set to 93 ANSI, ANSI or CCITT, and the DS3 signal is received from a DSX-3 OUT point. If the DS3 signal is received from a DSX-3 MONITOR point, set the MISC-PULSE MASK auxiliary function to NONE to prevent any confusion at seeing a *PULSE SHAPE FAIL* message.

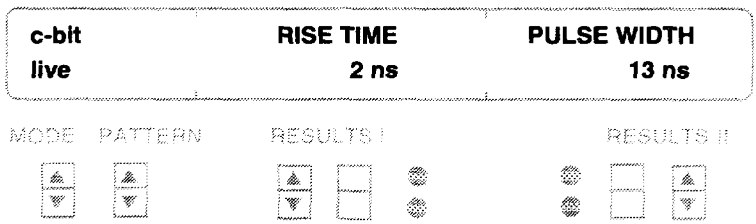
3. **Press the AUX switch (LED off) to exit the auxiliary functions**

4. **Connect the DS3 RECEIVE jack**

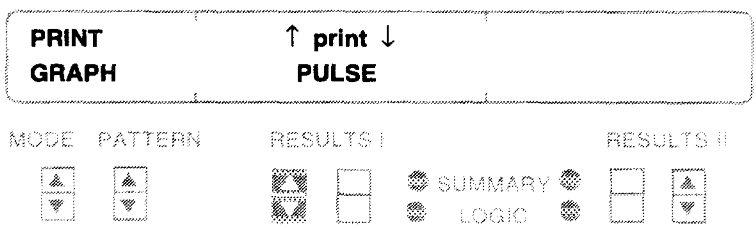
   Plug a cable between this jack and the span-side MONITOR jack.

5. **Verify the Primary DS3 Status LEDs**
   Verify the Signal Present LED illuminates.

6. **Verify the RESULTS I test results**
   Select the SIGNAL category and one of the following pulse shape results: PULSE WIDTH, RISE TIME, and FALL TIME. Scroll through the SIGNAL category pulse shape results to determine the pulse shape parameters. Refer to *Results Interpretation* for additional information concerning the results.



7. **Press the AUX switch (LED on) and set the following auxiliary functions:**
   Select the PRINT-GRAPH auxiliary function. Press the **RESULTS I** Results switch to generate the graph (see Figure 6-1). If a printer is not connected, the graph is stored in the print buffer.



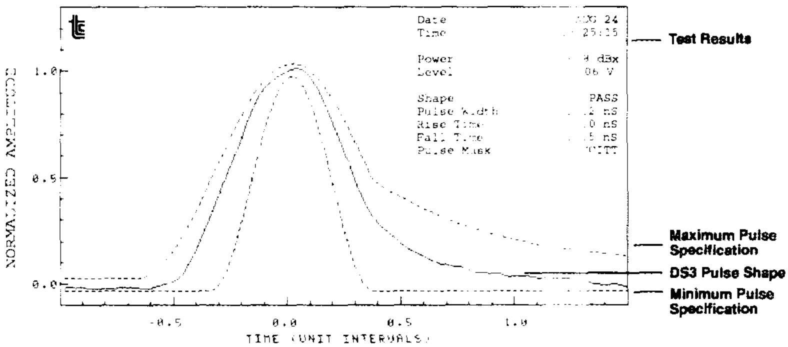


Figure 6-1
DS3 Pulse Shape Graph

8. Press the AUX switch (LED off) to exit the auxiliary functions

6.1.2 Results Interpretation

The signal measurements can be made periodically and compared to previous measurements. If a changing trend is noticed, the equipment can be checked and returned to normal before customers notice any problem on the line. The results are recorded in the results printouts. When monitoring a DS3 signal, observe the results in the SIGNAL category.

SIGNAL Category

PULSE WIDTH, RISE TIME, and FALL TIME — These results measure the pulse shape in nanoseconds between the 10% and 90% points for the rise time and fall time, and at the 50% points for the pulse width.

RX FREQ — The frequency of the clock recovered from the received data measured in Hz. The result also appears in the SUMMARY category if it is out of range.

POWER — The power level of the received DS3 signal measured in dBm.

LEVEL — The level of the received DS3 signal in volts peak.

OUT-OF-SERVICE DS3 PULSE SHAPE ANALYSIS

T-BERD 310 Mainframe Setup

Results Interpretation

6.2 OUT-OF-SERVICE DS3 PULSE SHAPE ANALYSIS

- Analyze the DS3 pulse shape against the pulse shape mask specified in either the ANSI T1.102-1991 standard, ANSI T1.102 1993 Standard, or the CCITT G.703 recommendation.
- Measure the DS3 pulse shape from a signal that contains isolated pulses (e.g., 2^23-1 or user-programmed 001 pattern) which is being received at the DS3 RECEIVE jack and from the DSX-3 level.
- Generate a pulse shape graph showing whether the pulse shape passed or failed against the selected pulse shape specification.

6.2.1 T-BERD 310 Mainframe Setup

1. **Loopback the far end**
   Loopback the far end of the DS3 span at the DSX-3 patch panel.

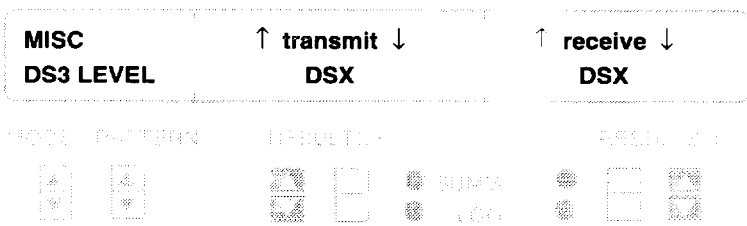
2. **RS-232 graphics-compatible printer**
   Connect the printer to the RS-232 interface. The printer must be set to accept an 8-bit character format.

3. **Set switches as follows:**

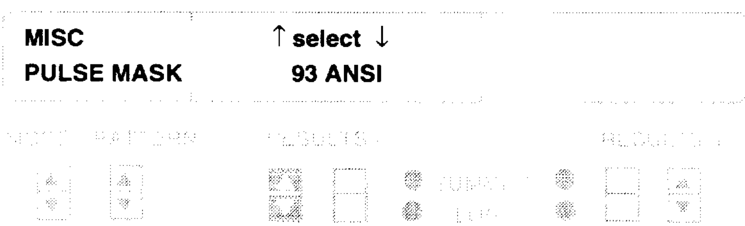
DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	M13, C-BIT, or UNFRAMED
PATTERN	2^23-1
Channel Control	DS3-DS1
DS3 TRANSMIT TIMING	INT

4. **Press the AUX switch (LED on) and set the following auxiliary functions:**

   a. Select the MISC-DS3 LEVEL auxiliary function to select the DSX transmit and receive level.



   b. Select the MISC-PULSE MASK auxiliary function to select the pulse mask.



NOTE: The 1993 ANSI Pulse Mask specification is not available in versions of software released prior to 1993. The more stringent ANSI selection may be used instead. This specification is from 1991 ANSI standards.

5. **Press the AUX switch (LED off) to exit the auxiliary functions**

6. **Connect the DS3 RECEIVE jack**

   Plug a cable between this jack and the span-side OUT jack.

7. **Connect the DS3 TRANSMIT jack**

   Plug a cable between this jack and the span-side IN jack.

8. Press the RESTART switch

Clear the old results and start a new test.

9. Verify Primary DS3 Status LEDs

These LEDs should illuminate: Signal Present, Frame Sync (if applicable), C-Bit Frame (if applicable), and Pattern Sync.

10. Press the RESULTS I Category switch

Select the SUMMARY category.

11. Press the ERROR INSERT switch and select DS3 LOGIC

12. Press the INSERT switch

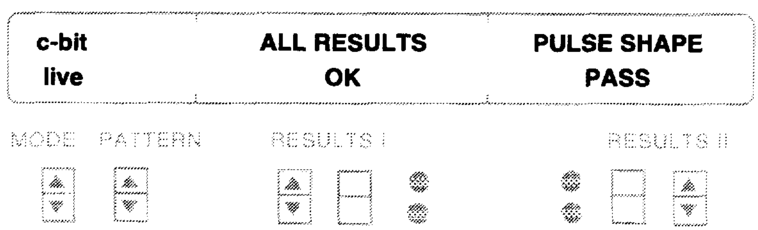
Press this switch quickly several times to send logic errors down the circuit. Verify the T-BERD 310 detects the errors and displays appropriate test results in the SUMMARY category. This verifies the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat the step.

13. Press the RESTART switch

Clear the old results and start a new test.

14. Verify the RESULTS II test results

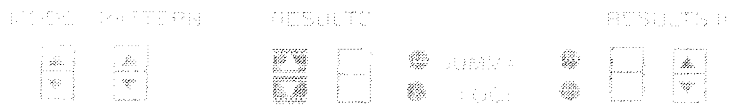
Select SIGNAL category and the PULSE SHAPE result. Refer to *Results Interpretation* for additional information concerning the results.



15. Press the AUX switch (LED on) and set the following auxiliary functions:

Select the PRINT-GRAPH auxiliary function. Press the **RESULTS I Results** switch to generate the graph (see Figure 6-1). If a printer is not connected, the graph is stored in the print buffer.

PRINT	**↑ print ↓**
GRAPH	**PULSE**



16. Press the AUX switch (LED off) to exit the auxiliary functions

6.2.2 Results Interpretation

The ANSI and CCITT pulse mask specifications are applicable only at the DSX-3 OUT point, and not at the DSX-3 monitor, HIGH, or LOW points. Since testing at the DSX-3 OUT point is an out-of-service test, the PULSE SHAPE PASS/FAIL result provides a convenient method to perform equipment verification during installation. When testing a DS3 pulse shape, observe the results in the SIGNAL category.

SIGNAL Category

PULSE WIDTH, RISE TIME, and FALL TIME — These results measure the pulse shape in nanoseconds between the 10% and 90% points for the rise time and fall time, and at the 50% points for the pulse width.
PULSE SHAPE — This result provides a simple PASS/FAIL indication which compares the signal pulse to either the ANSI or CCITT pulse mask specification selected through the MISC-PULSE MASK auxiliary function. By selecting a pulse mask, the T-BERD 310 can quickly indicate whether the signal pulses are within the selected pulse mask boundaries.

If the pulse shape results display the message *DENSITY ERR*, the signal being monitored does not contain enough isolated pulses to properly measure the pulse shape, try the 2^23-1 pattern.

The pulse shape graph includes the pulse mask, the pulse measurements, power and level readings, and indicates which pulse mask was selected. This hardcopy graph is an excellent tool to visually show that a signal is within specifications or to simplify record keeping.

DS3 JITTER

DS3 JITTER ANALYSIS

7.1 TESTING FOR DS3 WIDEBAND AND HIGHBAND JITTER

- Test for wideband and highband jitter to determine if it is affecting the DS3 circuit performance.
- Test results provide the current and maximum peak-to-peak wideband (10 Hz to 400 kHz) and highband (30 kHz to 400 kHz) jitter since initial signal presence or test restart. The results are expressed in peak-to-peak Unit Intervals (UIs).
- The demodulated jitter output, on the side panel, provides component information to measure the jitter amplitude and frequency with a spectrum analyzer.
- This test requires the 310-5 DS3 Jitter Option.

7.1.1 T-BERD 310 Mainframe Setup

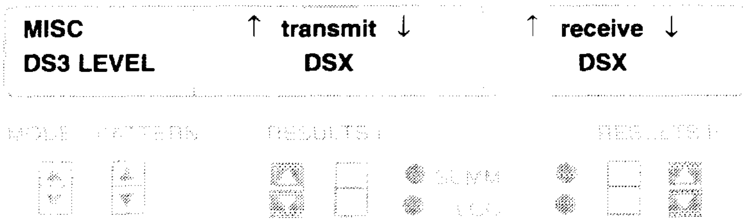
1. Set switches as follows:

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	AUTO

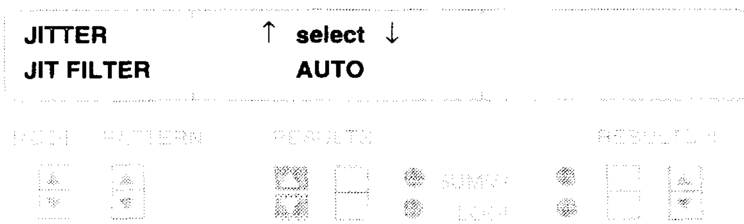
NOTE: The DS3 jitter analysis can only be performed from the DS3 RECEIVE jack.

2. **Press the AUX switch (LED on) and set the following auxiliary functions:**

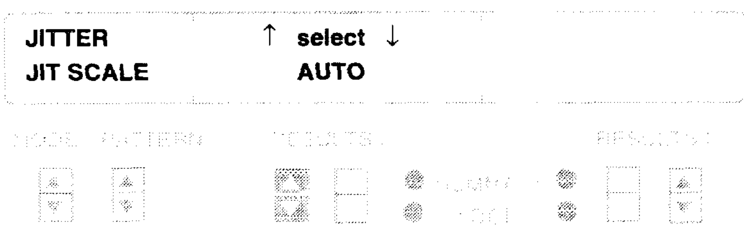
   a. Select the MISC-DS3 LEVEL auxiliary function to select the DSX transmit and receive level.



   b. Select the JITTER-JIT FILTER auxiliary function to set the filter bandwidth. AUTO alternates between the highband and wideband filters to monitor both frequency ranges.

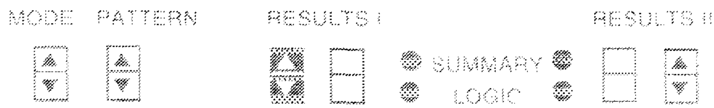


   c. Select the JITTER-JIT SCALE auxiliary function to set the jitter amplitude scale.



d. Select the JITTER-JIT THRESH auxiliary function to set the jitter test result threshold.

JITTER	**↑ select ↓**
JIT THRESH	**5.0 UI**



3. Press the AUX switch (LED off) to exit the auxiliary functions

4. Connect the DS3 RECEIVE jack

Plug a cable between this jack and the span-side MONITOR jack.

5. Press the RESULTS I Category switch

Select the SUMMARY category. If the jitter test results exceed the jitter threshold set in the JIT-JITTER THRESH auxiliary function, the test results appear in the SUMMARY category.

6 Press the RESTART switch

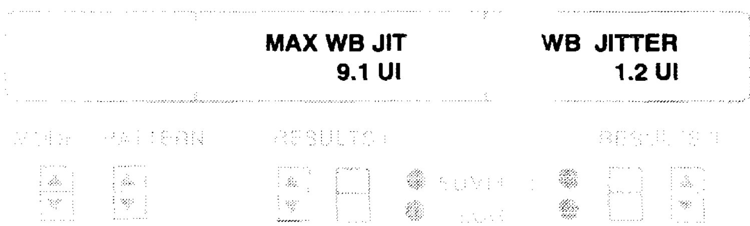
Clear the old results and start a new test.

7. Verify Primary DS3 Status LEDs

Verify the Signal Present LED illuminates.

8. Verify the RESULTS II test results

Select the SIGNAL category and the jitter results. Select the MAX WB JIT and WB JITTER to view the wideband jitter. Select the MAX HB JIT and HB JITTER to view the highband jitter. If the AUTO mode is selected in the jitter auxiliary functions, the associated results provide the necessary measurements that coincide with the selected filter and scale. Refer to *Results Interpretation* for additional information concerning the results.



9. Connect the JITTER OUTPUT jack (side panel)

Connect a spectrum analyzer to this jack. Determine exact jitter amplitudes and frequencies (optional).

7.1.2 Results Interpretation

The DS3 jitter measurements allow sources of jitter to be identified. When monitoring a DS3 signal for jitter, observe the results in the SIGNAL category.

SIGNAL Category

WB JITTER and MAX WB JIT — The wideband frequency bandwidth is 10 Hz to 400 kHz. Measure the wideband and maximum wideband jitter first. If unacceptable jitter is present, measure the highband and maximum highband jitter, to determine what frequency range is most affected.

HB JITTER and MAX HB JIT — The highband frequency bandwidth is 30 kHz to 400 kHz. If excess jitter is present in the highband results, the jitter could be caused by a number of accumulating sources such as along a regenerator span. If the highband readings do not indicate excess jitter, then the jitter is present in the lowband region (10 Hz to 30 kHz). Lowband jitter is usually caused by a single piece of equipment such as an M13 multiplexer.

M13 MULTIPLEXER (MULTIPLEX TEST)

DS3 MULTIPLEXER TESTING

8.1 M13 MULTIPLEXER (MULTIPLEX TEST)

- Verify the multiplexing functionality from the low-speed DS1 input to the high-speed DS3 output of a M13 multiplexer.
- Transmit a DS1 test pattern into each of the M13 multiplexer low-speed inputs.
- Perform DS3 testing on the M13 multiplexer output.
- Drop each DS1 channel from the DS3 signal and perform complete bit error rate analysis.
- This test requires the 310-1 DS1/DS0 Analyzer Option.

Figure 8-1 shows the T-BERD 310 connected to the low-speed DS1 channel input and the high-speed DS3 output of the M13 multiplexer.

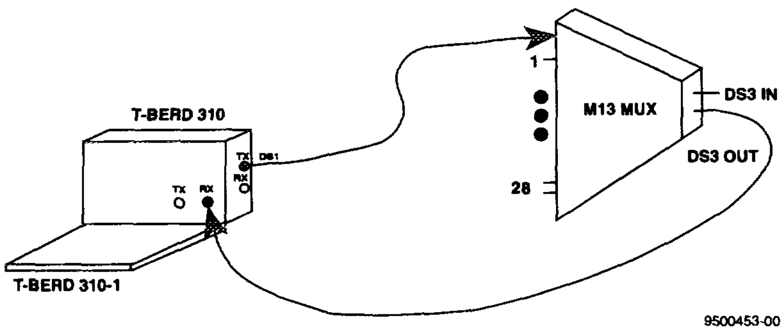


Figure 8-1
Testing the Multiplexing Capability of a DS3 Multiplexer

8.1.1 310-1 DS1/DS0 Analyzer Option Setup, Part 1

1. **Set switches as follows:**

DS1 SOURCE	DS3 DROP
MODE	T1 D4, T1 ESF, or T1
PATTERN	QRSS
TRANSMIT TIMING	INTERNAL

2. **Connect the DS1 TRANSMIT jack (side panel)**
   Plug a cable between this jack and one of the low-speed DS1 inputs of the DS3 multiplexer.

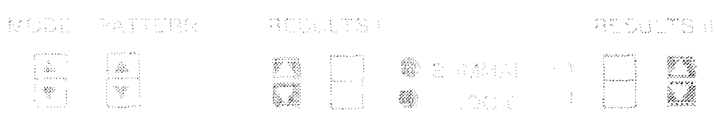
8.1.2 T-BERD 310 Mainframe Setup

3. **Set switches as follows:**

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	AUTO
Channel Control	DS3-DS1

4. **Press the AUX switch (LED on) and set the following auxiliary functions:**
   Select the MISC-DS3 LEVEL auxiliary function to select the HIGH receive level.

MISC	↑ **transmit** ↓	↑ **receive** ↓
DS3 LEVEL	**DSX**	**HIGH**

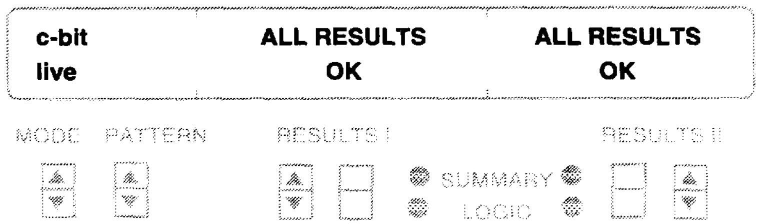


5. **Press the AUX switch (LED off) to exit the auxiliary functions**

6. **Connect the DS3 RECEIVE jack**
   Plug a cable between this jack and the DS3 output of the DS3 multiplexer.

7. **Verify Primary DS3 Status LEDs**
   These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync.

8. **Observe the MODE/PATTERN window**
   Verify the framing format and pattern.



NOTE: Since a muxed signal can be composed of many T1 patterns, the 310 treats muxed signals as live data.

9. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

10. **Press the DROP switch**
    Select the DS1 channel being dropped from the DS3 signal to the 310-1 DS1/DS0 Analyzer Option.

8.1.3 310-1 DS1/DS0 Analyzer Option Setup, Part 2

11. Press the RESTART switch
Clear the old results and start a new test.

12. Verify the Status LEDs
These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

13. Press the RESULTS I Category switch
Select the SUMMARY category.

14. Press the LOGIC ERROR INSERT switch
Press this switch quickly several times to send logic errors into the multiplexer. Verify the 310-1 detects the errors and displays appropriate test results in the SUMMARY category. This verifies the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat the step.

15. Press the RESTART switch
Clear the old results and start a new test.

16. Verify the RESULTS II test results
Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

8.1.4 Testing the Next DS1 Channel

17. Connect the DS1 TRANSMIT jack (side panel)

Plug the cable between this jack and the next low-speed DS1 input of the DS3 multiplexer.

18. T-BERD 310 DROP switch

Select the next DS1 channel being dropped from the DS3 signal to the 310-1 DS1/DS0 Analyzer Option.

19. Press the 310-1 RESTART switch

Clear the old results and start a new test.

20. Verify the 310-1 Status LEDs

These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

21. Verify the 310-1 RESULTS II test results

Refer to *310-1 Results Interpretation* for additional information concerning the results.

22. Test the next low-speed DS1 channel

Repeat Steps 17 through 21 to test all of the low-speed DS1 channels.

8.1.5 T-BERD 310 Results Interpretation

When monitoring the DS3 signal, observe the results in the BPV, PARITY, FRAME, and SIGNAL categories. Refer to Section 3.1 *Results Interpretation* to verify the DS3 signal is error free. Note the DS3 LOGIC category results are not applicable since the received signal contains multiplexed DS1 patterns and NOT a DS3 test pattern. Once the DS3 results are verified, the DS1 channel can be tested.

8.1.6 310-1 Results Interpretation

Except for the BPV category and the RX LVL dBdsx result (since the DS1 channel is internally dropped from the DS3 signal), the results for out-of-service DS1 BERT (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when testing the selected DS1 channel. When performing the test, observe the results in the LOGIC, FRAME, and SIGNAL categories.

M13 MULTIPLEXER (DEMULTIPLEX TEST)

T-BERD 310 Mainframe Setup, Part 1

310-1 DS1/DS0 Analyzer Option Setup, Part 1

T-BERD 310 Mainframe Setup, Part 2

310-1 DS1/DS0 Analyzer Option Setup, Part 2

T-BERD 310 Mainframe Setup, Part 3

310-1 Results Interpretation

8.2 M13 MULTIPLEXER (DEMULTIPLEX TEST)

- Verify the demultiplexing functionality from the high-speed DS3 input to the low-speed DS1 output of a M13 multiplexer.
- Transmit a multiplexed DS3 signal into the M13 multiplexer high-speed input.
- Perform complete bit error rate testing on each of the DS1 signals demultiplexed by the M13 multiplexer.
- This test requires the 310-1 DS1/DS0 Analyzer Option.

Figure 8-2 shows the T-BERD 310 connected to the low-speed DS1 channel output and the high-speed DS3 input of the M13 multiplexer.

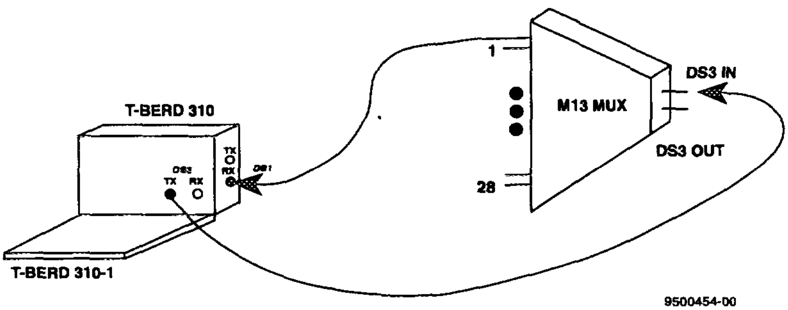


Figure 8-2
Testing the Demultiplexing Capability of a DS3 Multiplexer

8.2.1 T-BERD 310 Mainframe Setup, Part 1

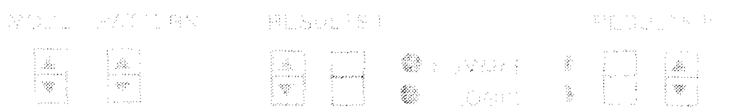
1. **Set switches as follows:**

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	MUXED M13 or MUXED C-BIT
PATTERN	channelized DS1 test pattern, e.g., T1D4 QRSS
Channel Control	DS3-DS1
DS3 TRANSMIT TIMING	INT

NOTE: The "— — —" appear in the INSERT window indicating that the pattern is not transmitted yet on any DS1 channel. An All Ones pattern is generated instead..

2. **Press the AUX switch (LED on) and set the following auxiliary functions:**
   Select the MISC-DS3 LEVEL auxiliary function to select the LOW transmit level.

MISC	**↑ transmit ↓**	**↑ receive ↓**
DS3 LEVEL	**LOW**	**DSX**



3. **Press the AUX switch (LED off) to exit the auxiliary functions**

4. **Connect the DS3 TRANSMIT jack**
   Plug a cable between this jack and the DS3 input of the M13 multiplexer.

8.2.2 310-1 DS1/DS0 Analyzer Option Setup, Part 1

5. Set switches as follows:

DS1 SOURCE	EXT. INPUT (DS1 from DS1 RECEIVE jack).
MODE	AUTO

6. Press the RECEIVE INPUT switch and connect DS1 RECEIVE jack (side panel)

Select the TERM input level and plug a cable between this jack and the DS1 channel output being tested.

8.2.3 T-BERD 310 Mainframe Setup, Part 2

7. Press the INSERT switch

Select the DS1 channel being tested. The selected DS1 channel contains the selected test pattern (see Step 1). The other DS1 channels contain an All Ones pattern.

8.2.4 310-1 DS1/DS0 Analyzer Option Setup, Part 2

8. Press the RESTART switch

Clear the old results and start a new test.

9. Verify the Status LEDs

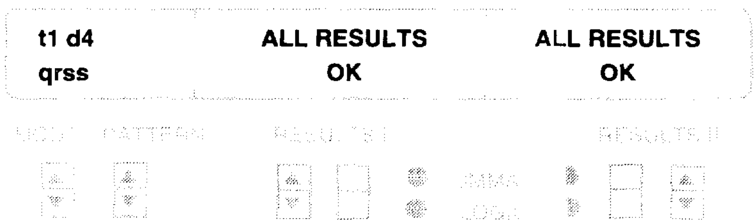
These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

10. Verify the Alarm LEDs

These LEDs should not be illuminated. If the All Ones LED illuminates, verify the T-BERD 310 is connected properly and the **INSERT** switch is set properly.

11. Observe the MODE/PATTERN window

Verify the framing format and pattern. The framing format and test pattern must match the framing format and test pattern shown in the T-BERD 310 display..



12. Verify the RESULTS I test results

Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

8.2.5 T-BERD 310 Mainframe Setup, Part 3

13. Press the ERROR INSERT switch and select DS3 LOGIC

14. Press the Error INSERT switch

Press this switch quickly several times to send logic errors down the circuit. Verify the 310-1 detects the errors and displays appropriate test results in the SUMMARY category. This verifies the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat this step.

NOTE: Some T-BERD 310s may not be equipped with this capability. The LOGIC error insert may randomly select a location within the DS3 to insert the error, rather than the DS1 channel. To determine if the T-BERD 310 is equipped with this feature, loop the DS3 RECEIVER jack to the DS3 TRANSMITTER jack. Select a Muxed M13 or Muxed C-Bit Mode. Press the **ERROR INSERT** switch once. If the error is displayed in the SUMMARY category of the mainframe, the T-BERD 310 is not inserting the error on the DS1 signal. (A simple factory upgrade can be performed to add this capability.) If the error is not reported on the mainframe, the error is located on the DS1 channel selected by the **Channel Control INSERT** switch and will be visible at a DS1 test access point.

15. Test the next low-speed DS1 channel

Repeat Steps 6 through 15 to test the other low-speed DS1 channels.

8.2.6 310-1 Results Interpretation

All DS1 results for out-of-service DS1 BERT testing (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when testing the demultiplexing functionality. When performing an out-of-service DS1 bit error rate test, observe the results in the LOGIC, BPV, FRAME, and SIGNAL categories.

Testing the demultiplexing functionality of an M13 multiplexer involves transmitting a multiplexed DS3 test signal into the multiplexer DS3 input. The transmitted DS3 test signal (MUXED M13 or MUXED C-BIT) contains 28 multiplexed DS1 test patterns and the proper DS1, DS2, and DS3 framing and overhead bits to allow the multiplexer to receive and demultiplex the DS3 test signal into the 28 DS1 channels.

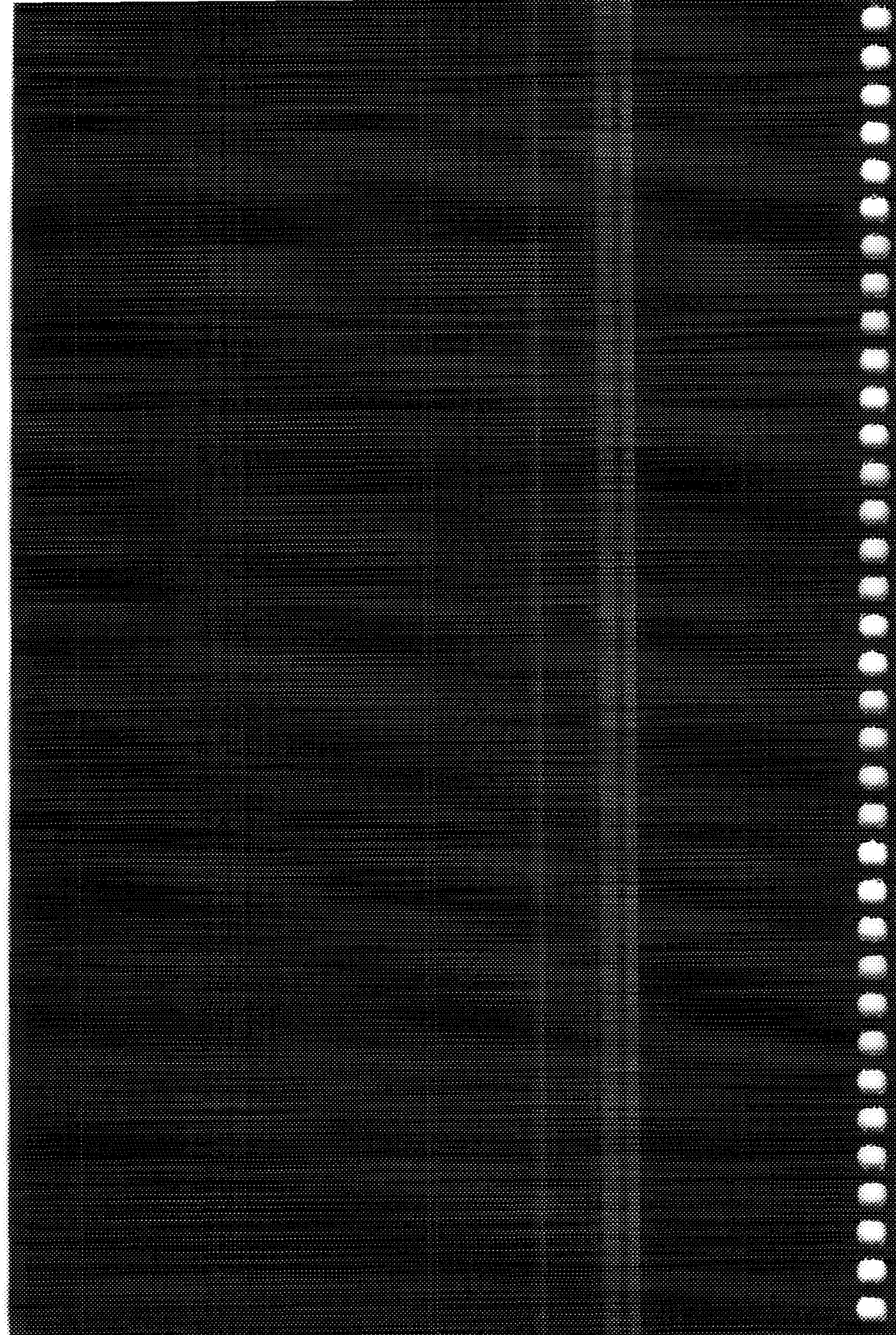
The selected DS1 test pattern can be inserted into ALL 28 DS1 channels, or into only one selected DS1 channel with the remaining 27 DS1 channels containing an ALL ONES pattern. Inserting the DS1 pattern into only one DS1 channel allows each DS1 to be isolated and verification the multiplexer is demultiplexing each DS1 to the proper DS1 output.

M13 MULTIPLEXER (MULTIPLEX/DEMULTIPLEX TEST)

Network Configuration

310-1 DS1/DS0 Analyzer Option Setup

310-1 Results Interpretation



8.3 M13 MULTIPLEXER (MULTIPLEX/DEMULTIPLEX TEST)

- Perform bit error rate test between the low-speed DS1 ends of a DS3 network.
- Verify the multiplexing/demultiplexing functionality of the M13 multiplexers.
- This test requires the 310-1 DS1/DS0 Analyzer Option.

Figure 8-3 shows the T-BERD 310 connected to the near-end low-speed DS1 side of a M13 multiplexer and the far-end low-speed DS1 side looped back.

8.3.1 Network Configuration

1. **Daisy chain the near-end DS1 channels**
   Connect the output of Channel 1 to the input of Channel 2, the output of Channel 2 to the input of Channel 3, etc. The input for Channel 1 and the output for Channel 28 should be open.

2. **Loopback the far-end DS1 channels**
   Loopback all 28 DS1 channels manually, with cables.

8.3.2 310-1 DS1/DS0 Analyzer Option Setup

3. **Set switches as follows:**

DS1 SOURCE	EXT. INPUT (side-panel DS1 RECEIVE jack).
MODE	T1 D4, T1 ESF, or T1
PATTERN	QRSS
TRANSMIT TIMING	INTERNAL
CODE	AMI or B8ZS
RECEIVE INPUT	TERM

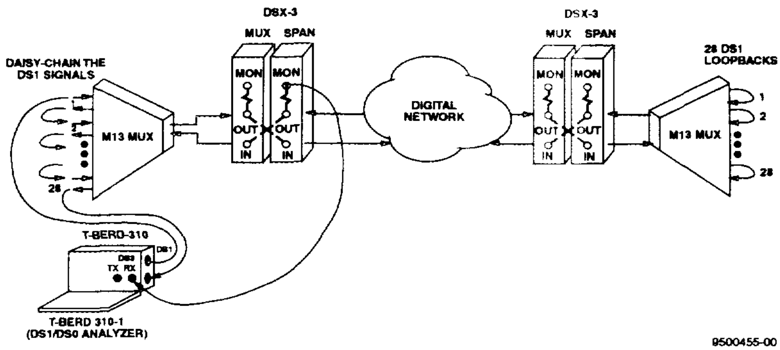


Figure 8-3
Testing the DS3 Multiplexing/Demultiplexing Capability

4. **Connect the DS1 RECEIVE jack (side panel)**
   Plug a cable between this jack and the low-speed output for DS1 channel 28.

5. **Connect the DS1 TRANSMIT jack (side panel)**
   Plug a cable between this jack and the low-speed input for DS1 channel 1.

6. **Press the RESTART switch**
   Clear the old results and start a new test.

7. **Verify the Status LEDs**
   These LEDs should illuminate: T1 Pulses, Frame Sync, Pattern Sync, and B8ZS (if applicable).

8. **Verify the RESULTS I Category switch**
   Select the SUMMARY category.

9. **Press the LOGIC ERROR INSERT switch**

   Press this switch quickly several times to send logic errors down the circuit. Verify the 310-1 detects the errors and displays appropriate test results in the SUMMARY category. This verifies the transmitted signal is being looped back and received. If the errors are not detected, verify the far-end loopback and repeat this step.

10. **Press the RESTART switch**

    Clear the old results and start a new test.

11. **Verify the RESULTS II test results**

    Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

8.3.3 310-1 Results Interpretation

All DS1 results for out-of-service DS1 BERT testing (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when testing the multiplexing/demultiplexing functionality of the network. When performing an out-of-service DS1 bit error rate test, observe the results in the LOGIC, BPV, FRAME, and SIGNAL categories. This application allows multiplexing and demultiplexing testing of each M13 multiplexer while also testing the integrity of the full end-to-end transmission path using only a single DS1 transmitter and receiver.

DCS 3/3 TESTING

T-BERD 310 Mainframe Setup

Results Interpretation

DIGITAL CROSS-CONNECT TESTING

9.1 DCS 3/3 TESTING

- Verify the DCS 3/3 cross-connect mapping.

Figure 9-1 illustrates the test setup with the T-BERD 310 connected to the DCS 3/3.

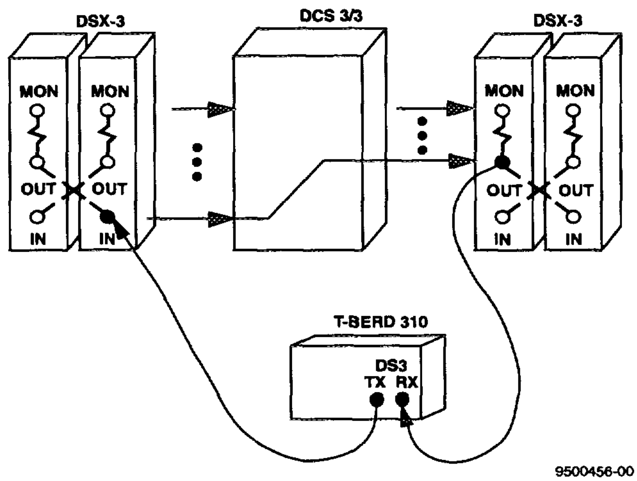


Figure 9-1
Setting Up for DCS 3/3 Testing

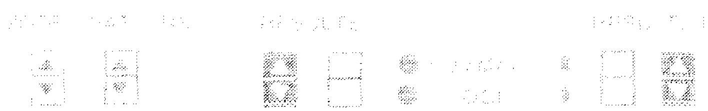
9.1.1 T-BERD 310 Mainframe Setup

1. **Set switches as follows:**

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	M13 or C-BIT
PATTERN	2^23-1
DS3 TRANSMIT TIMING	INT

2. **Press the AUX switch (LED on) and set the following auxiliary functions:**
   Select the MISC-DS3 LEVEL auxiliary function to select the DSX or LOW (for < 200 feet) transmit level and DSX receive level.

MISC	**↑ transmit ↓**	**↑ receive ↓**
DS3 LEVEL	**DSX**	**DSX**



3. **Press the AUX switch (LED off) to exit the auxiliary functions**

4. **Connect the DS3 RECEIVE jack**
   Plug a cable between this jack and the DS3 East-side OUT jack.

5. **Connect the DS3 TRANSMIT jack**
   Plug a cable between this jack and the DS3 West-side IN jack.

6. **Press the RESTART switch**
   Clear the old results and start a new test.

7. **Verify Primary DS3 Status LEDs**
   These LEDs should illuminate: Signal Present, Frame Sync, Pattern Sync, and C-Bit Frame (if applicable).

8. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *Results Interpretation* for additional information concerning the results.

9. **Press the ERROR INSERT switch and select DS3 LOGIC**

10. **Press the INSERT switch**
    Press this switch several times to verify the cross-connect mapping, these errors should appear in the SUMMARY category.

9.1.2 Results Interpretation

The DS3 test pattern is transmitted into a DCS DS3 input, and received through the mapped DCS DS3 output to the T-BERD 310. If the DS3 signal is mapped correctly through the DCS 3/3, the T-BERD 310 indicates frame and pattern synchronization. The results for out-of-service DS3 BERT testing (see Section 4.1) and in-service DS3 monitoring (see Section 3.1) are applicable when testing the DCS DS3 signal. When performing the test, observe the results in the LOGIC, BPV, PARITY, FRAME, and SIGNAL categories.

DCS 3/1 TESTING

9.2 DCS 3/1 TESTING

- Verify the DCS 3/1 cross-connect mapping.
- This test requires the 310-1 DS1/DS0 Analyzer Option.

Figure 9-2 illustrates the test setup with the T-BERD 310 connected to the DCS 3/1.

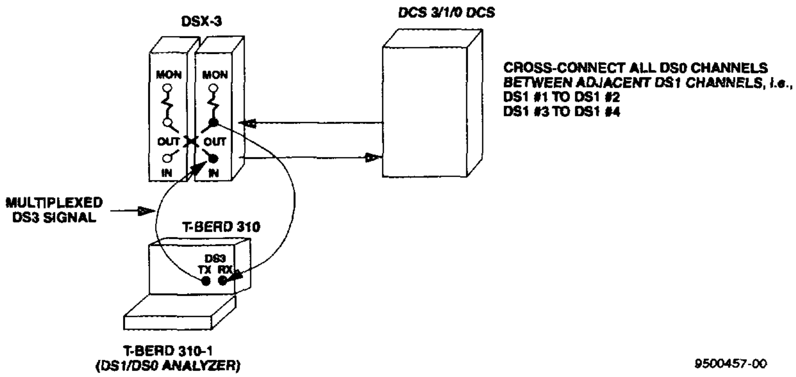


Figure 9-2
Setting Up for DCS 3/1 Testing

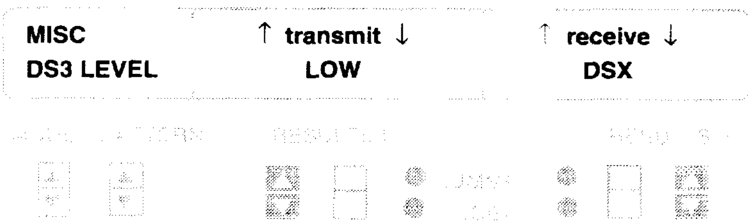
9.2.1 T-BERD 310 Mainframe Setup

1. **Set switches as follows:**

DS3 SOURCE	EXT (DS3 RECEIVE jack)
Setup	DS3
MODE	MUXED M13 or MUXED C-BIT
PATTERN	channelized DS1 test pattern, e.g., T1D4 QRSS
Channel Control	DS3-DS1
DS3 TRANSMIT TIMING	INT

NOTE: The "— — —" appear in the INSERT window indicating that an All Ones pattern is being inserted on each T1.

2. **Press the AUX switch (LED on) and set the following auxiliary functions:**
   Select the MISC-DS3 LEVEL auxiliary function to select the DSX for the transmit and receive level.



3. **Press the AUX switch (LED off) to exit the auxiliary functions**

4. **Connect the DS3 RECEIVE jack**
   Plug a cable between this jack and the DS3 East-side OUT jack.

5. **Connect the DS3 TRANSMIT jack**
   Plug a cable between this jack and the DS3 West-side IN jack.

6. **Press the RESTART switch**
   Clear the old results and start a new test.

7. **Verify the Primary DS3 Status LEDs**
   These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), and DS2 Frame Sync.

8. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

9.2.2 310-1 DS1/DS0 Analyzer Option Setup

9. Press the DS1 SOURCE switch
Select DS3 DROP (DS1 dropped from T-BERD 310).

10. Press the MODE switch
Select AUTO.

9.2.3 Verifying the DS1 Channel Mapping

11. Press the INSERT switch
Insert the test pattern into the first mapped DS1 channel.

12. Press the DROP switch
Drop the first mapped DS1 channel.

NOTE: If three dots appear in the dropped channel, the 310 is detecting an AIS on this signal.

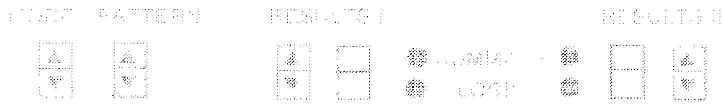
13. Press the 310-1 RESTART switch
Clear the old results and start a new test.

14. Verify the 310-1 Status LEDs
These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync.

15. Verify the 310-1 Alarm LEDs
These LEDs should not be illuminated. If the All Ones LED illuminates, check the DS1 mapping and the selected channels.

16. Observe the 310-1 MODE/PATTERN window
Verify the framing format and pattern. The indicated framing format and pattern should match the framing format and pattern selected in Step 1, e.g., T1D4 QRSS.

t1 d4	ALL RESULTS	BIT ERRORS
qrss	OK	0



17. Verify the 310-1 RESULTS I test results

Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310-1 Results Interpretation* for additional information concerning the results.

18. Repeat Steps 11 to 17 to verify the next mapped DS1 channel

9.2.4 T-BERD 310 Results Interpretation

Testing the DCS 3/1 mapping involves transmitting a multiplexed DS3 test signal into the DCS DS3 input. The transmitted DS3 test signal (MUXED M13 or MUXED C-BIT) contains 28 multiplexed DS1 test patterns and the proper DS1, DS2, and DS3 framing and overhead bits to allow the DCS 3/1 to receive and redirect the DS1 channels into the appropriately mapped DS3 output. The T-BERD 310 receives the DS3 output and drops the DS1 test pattern to the 310-1 DS1/DS0 Analyzer Option.

If the DCS DS3 signals have been mapped correctly, the T-BERD 310 indicates DS3 frame synchronization (Frame Sync LED illuminates).

9.2.5 310-1 Results Interpretation

Except for the BPV category and the RX LVL dBdsx result (since the DS1 channel is internally dropped from the DS3 signal), the results for out-of-service DS1 BERT testing (see Section 4.2) and in-service DS1 monitoring (see Section 3.3) are applicable when verifying the DCS 3/1 mapping. When performing an out-of-service DS1 bit error rate test from a DS3 access point, observe the results in the LOGIC, FRAME, and SIGNAL categories.

The selected DS1 test pattern can be inserted into ALL 28 DS1 channels, or into only one selected DS1 channel with the remaining 27 DS1 channels containing an ALL ONES pattern. Inserting the DS1 pattern into only one DS1 channel allows each DS1 to be isolated and verified the DCS 3/1 is mapping each DS1 channel from the proper DS3 input and to the proper DS3 output.

If the DCS DS1 signals have been mapped correctly, the T-BERD 310-1 indicates DS1 frame and pattern synchronization to the DS1 signal (Frame Sync LED and Pattern Sync LED illuminate).

SONET

MONITORING STS-1 OR OC-N SIGNALS AND DS3 OR DS1 PAYLOADS

SONET TESTING

10.1 MONITORING STS-1 OR OC-N SIGNALS AND DS3 OR DS1 PAYLOADS

- Evaluate the SONET STS-1 or OC-n (n is 1, 3, or 12) performance while dropping and analyzing a DS3 or DS1 payload from the SONET signal.
- Requires the 310-1 and either the 310-12, 310-13R, or 310-14R option.

Figure 10-1 illustrates how the T-BERD 310 connects to the SONET circuit to analyze SONET overhead and a DS3 or DS1 payload. The following application is divided into three parts:

- T-BERD 310 SONET Receiver Setup and Analysis
- T-BERD 310 DS3 Receiver Setup and Analysis
- 310-1 DS1 Receiver Setup and Analysis

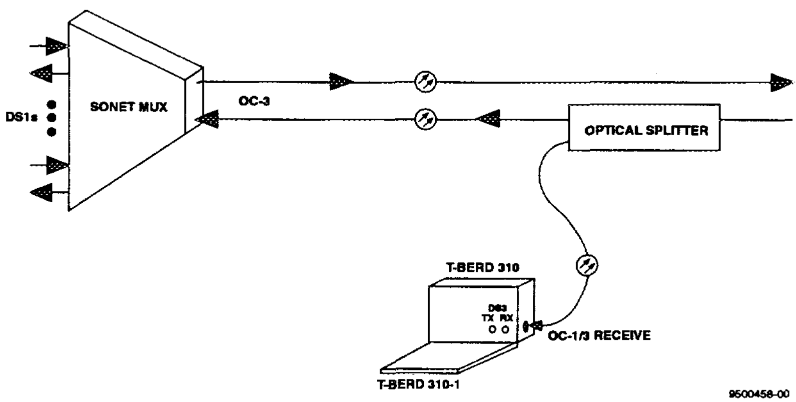


Figure 10-1
Setup for Monitoring SONET Signals and a DS3 or DS1 Payload

10.1.1 T-BERD 310 SONET Receiver Setup and Analysis

1. **Set switches as follows to select the STS:**

Setup	SONET RX
RATE	STS-1, OC-1, OC-3, or OC-12
PAYLOAD	AUTO (see following table for additional selections)
Channel Control	SONET-STS
DROP	OC-3, 1 to 3 or OC-12, 1 to 12

2. **Set switches as follows to select the VT:**

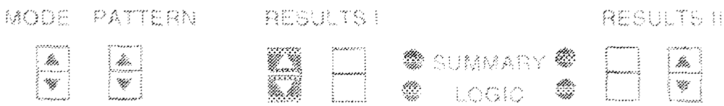
Channel Control	SONET-VT
DROP	Sequential, 1 to 28 or GP/VT, 1,1 to 7,4

Payload	AUTO	DS3 ASYN	DS1 ASYN	DS1 BIT	DS1 BYTE
DS1 Channel	DS3, N/A DS1, 1 to 28	—	1 to 28	1 to 28	1 to 28
Drop To	DS3, 310 DS1, 310-1	310	310-1	310-1	310-1

3. **Press the AUX switch (LED on) and set the following auxiliary function:**

   When testing an STS-1 signal, select the SONET RX-STS RX LEVEL auxiliary function and set the STS-1 signal input level.

SONET RX	**↑ select ↓**
STS RX LEVEL	**DSX**



4. **Press the AUX switch (LED off) to exit the auxiliary functions**

5. **Connect a SONET source to the T-BERD 310**

   Connect a SONET cable to the desired side-panel connection:

   - STS-1 RECEIVE
   - OC-1/OC-3 RECEIVE
   - OC-12 RECEIVE

   NOTE: Clean optical connections with denatured alcohol before attaching them to the T-BERD 310 optical connectors.

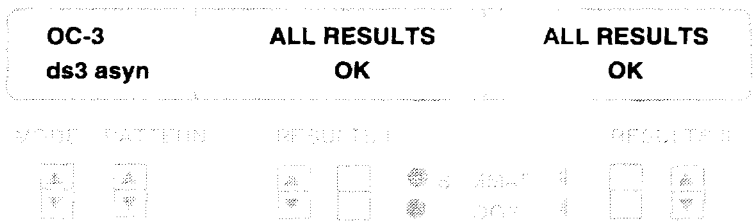
6. **Press the RESTART switch**

   Clear the old results and start new test.

7. **Verify the SONET Status LEDs**

   The SONET Signal Present, Frame Sync, Path PTR Pres, and VT PTR Pres (if applicable) LEDs should illuminate indicating a valid framed SONET signal. For optical inputs on the 310-12 and 310-14R options, verify the side-panel LED above either OC-1/OC-3 RECEIVE or OC-12 RECEIVE optical connector illuminates when the cable is connected indicating a signal is detected.

8. **Observe the SONET RATE/PAYLOAD window**
   Verify the received rate and detected payload.



9. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected in the SONET overhead, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *SONET Results Interpretation* for additional information concerning the results. Note any SONET alarms indicated on the front panel or in the SUMMARY category as follows:

LOS	Loss of Signal alarm
LOF	Loss of Frame alarm
SEF	Severely Errored Frame alarm
LINE AIS	Line alarm indication signal (AIS) alarm
LINE RDI	Line remote defect indication (RDI) alarm (also known as FERF)
PATH AIS	Path AIS alarm
PATH RDI	Path RDI alarm (also known as RAI or Yellow Alarm)
PATH LOP	Path loss of pointer (LOP) alarm
VT AIS	VT AIS alarm
VT RDI	VT RDI alarm (also known as RAI or Yellow Alarm)
VT LOP	VT LOP alarm

10.1.2 SONET Results Interpretation

The T-BERD 310 monitors the SONET signal overhead information and presents the test results in the SONET categories (SECTION, LINE, PATH, and VT) as follows:

SECTION Category

FRM WORD ERR and SON SEF SEC — Frame Word Errors and SONET Severely Errored Frame Seconds indicate incorrect framing bits are being generated by the SONET equipment or corrupted during transmission.

SECT BIP ERR and SECT EQU BER — Bit interleave parity errors indicate the data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

SONET RX FREQ — The SONET received frequency measurement verifies the received SONET signal frequency in Hertz. If the result is out of specification, it appears in the SUMMARY category.

LINE Category

POINTER JUST, POINTER INC, POINTER DEC, POINTER NDF, and POINTER DATA — Line pointer justification results monitor for excessive changes in the SPE payload pointer, which indicates a network timing problem between SONET nodes.

APS MSG CNT, APS INFO, and APS CONFIG — Automatic protection switching results indicate the number of APS messages that have been received, the last APS message received, and the APS configuration.

LINE UAS— Measures the total unavailable seconds due to excessive bit errors, loss of pointer, or AIS condition. The result appears in the SUMMARY category when an error exists.

LINE BIP ERR and LINE EQU BER — Bit interleave parity errors indicate the data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

PATH Category

PATH TRACE — The Path Trace result determines the origin of the signal and is a convenient method of determining path connectivity.

PATH UAS — Measures the total unavailable seconds due to excessive bit errors, loss of pointer, or AIS condition. The result appears in the SUMMARY category when an error exists.

PATH BIP ERR and PATH EQU BER — Bit interleave parity errors indicate the data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

VT Category

VT UAS — Measures the total unavailable seconds due to excessive bit errors, loss of pointer, or AIS condition. The result appears in the SUMMARY category when an error exists.

VT BIP ERR and VT EQU BER — Bit interleave parity errors indicate the data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

VT PTR JUST, VT PTR INC, VT PTR DEC, VT PTR NDF, and VT PTR DATA — VT pointer justification results monitor for excessive changes in the VT payload pointer, which indicates a network timing problem between SONET nodes.

10.1.3 T-BERD 310 DS3 Receiver Setup and DS3 Payload Analysis

Perform the following procedure to analyze a DS3 payload dropped from a SONET signal.

1. **Set switches as follows:**

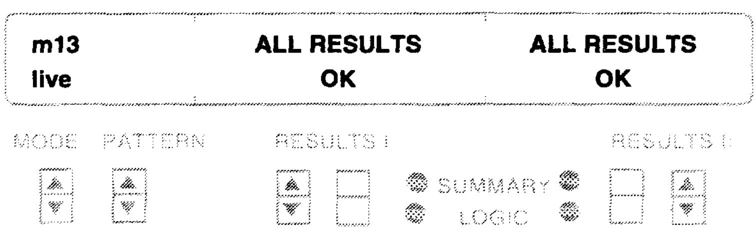
DS3 SOURCE	SONET
Setup	DS3
MODE	AUTO

NOTE: If the DS3 signal is properly framed (DS2 and DS1 framing), DS1 or E1 channels can also be dropped and monitored. The DS1 channels can be dropped to either the 310-1 DS1/DS0 Analyzer Option or DS1 DROP jack (side panel) and an external DS1 test set. The E1 channels can be dropped to the E1 DROP jack (side panel) and an external E1 test set.

2. **Press the RESTART switch**
   Clear the old results and start new test.

3. **Verify the Primary DS3 Status LEDs**
   These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), DS2 Frame Sync (if applicable), and Pattern Sync (if applicable).

4. **Verify the framing format and pattern in the MODE/PATTERN window**



5. **Verify the RESULTS I test results**

   Select the SUMMARY category. If no errors are detected in the DS3 payload, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

10.1.4 T-BERD 310 Results Interpretation

The BPV and SIGNAL category test results (except RX FREQ) are not applicable for this application since the DS3 signal is generated by the T-BERD 310. Refer to Section 3.1 for applicable in-service test results.

10.1.5 310-1 DS1 Receiver Setup and DS1 Payload Analysis

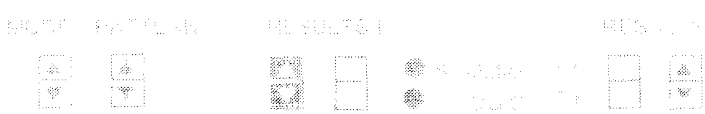
Perform the following procedure to analyze a DS1 payload dropped from a SONET signal when the T-BERD 310 indicates *ds1 asyn* or *ds1 byte* mapping.

1. **Press the DS1 SOURCE switch and select SONET DROP**

2. **Press the AUX switch (LED on) and set the following auxiliary functions:**

   Select the MISC-DS1 SIG BITS auxiliary function, and set the DS1 signaling transfer mode.

MISC	**↑ select ↓**
DS1 SIG BITS	**PASS-THRU**



NOTE: This allows DS1 signaling bits to pass through the SONET receiver without being altered. The selection is only applicable with byte-synchronous mapping.

3. **Press the MODE switch and select AUTO**

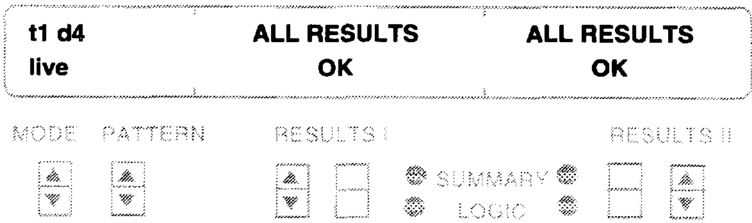
4. **Press the RESTART switch**

   Clear the old results and start a new test.

5. **Verify the 310-1 Status LEDs**

   These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync (if applicable).

6. **Verify the framing format and pattern in the 310-1 MODE/PATTERN window**



7. **Verify the 310-1 RESULTS I test results**

   Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

10.1.6 310-1 Results Interpretation

When monitoring a DS1 payload from a SONET signal, observe the results in the FRAME and SIGNAL categories.

NOTE: The BPV category and RX LVL dBdsx result are not applicable since the DS1 channel is dropped internally from within a SONET signal.

FRAME Category

Frame error results — Since the DS1 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS1 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.

CRC error results (ESF framing only) — CRC errors indicate the integrity of the line at any error rate.

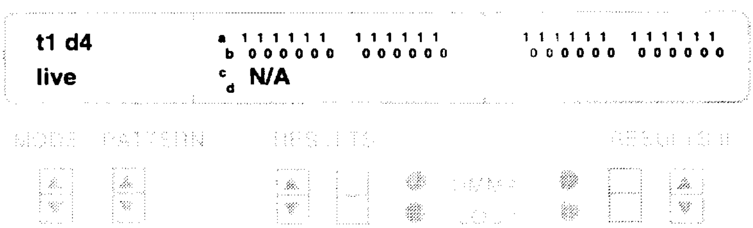
SIGNAL Category

The SIGNAL category results include both DS1 and DS0 measurements.

RX FREQ — The DS1 received frequency result is pertinent to DS1 signal processing. Note that if the received frequency is out of specification (< 1,543,923 or > 1,544,077 Hz), the result automatically appears in the SUMMARY category.

VF LVL dBm — The DS0 channel VF level can be measured while listening to the voice channel on the internal speaker.

abcd — The ABCD signaling bits are pertinent to DS0 channel signaling. The ABCD Signaling Bits result shows signaling bits for all 24 DS0s simultaneously, and provides an easy method to locate an active channel. The active channel can then be selected and listened to on the internal speaker.



TESTING LOW-SPEED (DS3/DS1) TO HIGH-SPEED (SONET) CIRCUITS

10.2 TESTING LOW-SPEED (DS3/DS1) TO HIGH-SPEED (SONET) CIRCUITS

- Test SONET multiplexer (SM), add/drop multiplexer (ADM), or digital cross-connect system (DCS) circuit functionality from the low-speed DS1 or DS3 side to the high-speed SONET STS-1 or OC-n (n is 1, 3, or 12) side while dropping and analyzing the DS3 or DS1 payload from the SONET signal.

- Requires the 310-1 and either the 310-12, 310-13R, or 310-14R option.

Figure 10-2 illustrates how the T-BERD 310 connects to the SONET circuit to analyze SONET overhead and a DS3 or DS1 payload. The following application is divided into five parts:

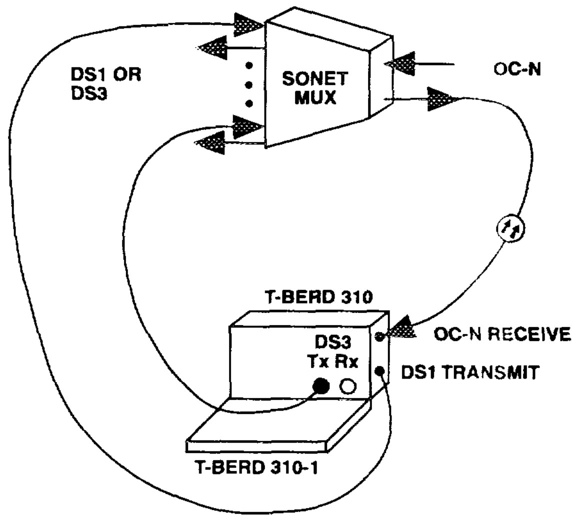
- T-BERD 310 SONET Receiver Setup and Analysis

- T-BERD 310 DS3 Transmitter Setup

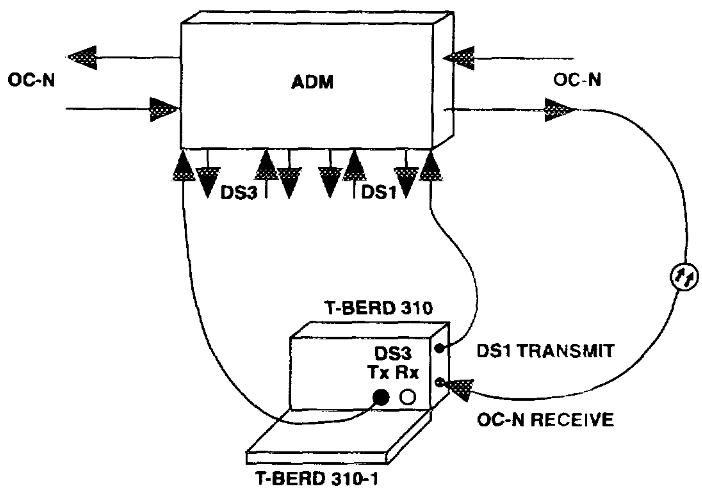
- 310-1 DS1 Transmitter Setup

- T-BERD 310 DS3 Receiver Setup and Analysis

- 310-1 DS1 Receiver Setup and Analysis



TESTING SONET MULTIPLEXERS (LOW- TO HIGH-SPEED)



TESTING ADD/DROP MULTIPLEXERS (LOW- TO HIGH-SPEED)

9500459-00

Figure 10-2
Setup for Testing Low- to High-Speed SONET Circuits

10.2.1 T-BERD 310 SONET Receiver Setup

1. **Set switches as follows to select the STS:**

Setup	SONET RX
RATE	STS-1, OC-1, OC-3, or OC-12
PAYLOAD	AUTO (see following table for additional selections)
Channel Control	SONET-STS
DROP	OC-3, 1 to 3 or OC-12, 1 to 12

2. **Set switches as follows to select the VT:**

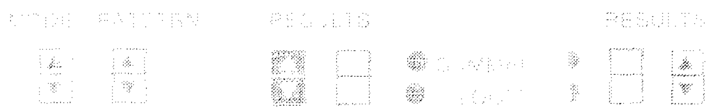
Channel Control	SONET-VT
DROP	Sequential, 1 to 28 or GP/VT, 1,1 to 7,4

Payload	AUTO	DS3 ASYN	DS1 ASYN	DS1 BIT	DS1 BYTE
DS1 Channel	DS3, N/A DS1, 1 to 28	—	1 to 28	1 to 28	1 to 28
Drop To	DS3, 310 DS1, 310-1	310	310-1	310-1	310-1

3. **Press the AUX switch (LED on) and set the following auxiliary function:**

   When testing an STS-1 signal, select the SONET RX-STS RX LEVEL auxiliary function and set the STS-1 signal input level.

SONET RX	↑ select ↓
STS RX LEVEL	DSX



4. **Press the AUX switch (LED off) to exit the auxiliary functions**

5. **Connect a SONET source to the T-BERD 310**

   Connect a SONET cable to the desired side-panel connection:

   - STS-1 RECEIVE
   - OC-1/OC-3 RECEIVE
   - OC-12 RECEIVE

   NOTE: Clean optical connections with denatured alcohol before attaching them to the T-BERD 310 optical connectors.

6. **Press the RESTART switch**

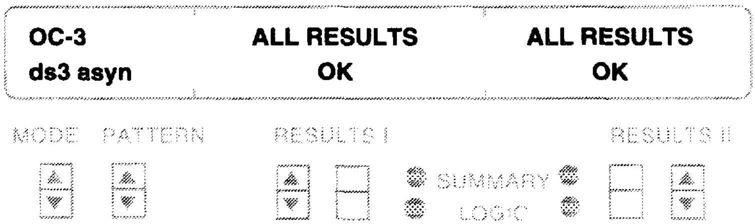
   Clear the old results and start new test.

7. **Verify the SONET Status LEDs**

   The SONET Signal Present, Frame Sync, Path PTR Pres and VT PTR Pres (if applicable) LEDs should illuminate indicating a valid framed SONET signal. For optical inputs on the 310-12 and 310-14R options, verify the side-panel LED above either OC-1/OC-3 RECEIVE or OC-12 RECEIVE optical connector illuminates when the cable is connected indicating a signal is detected.

8. Observe the SONET RATE/PAYLOAD window

Verify the received rate and detected payload.



9. Verify the RESULTS I test results

Select the SUMMARY category. If no errors are detected in the SONET overhead, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *SONET Results Interpretation* for additional information concerning the results. Note any SONET alarms indicated on the front panel or in the SUMMARY category as follows:

LOS	Loss of Signal alarm
LOF	Loss of Frame alarm
SEF	Severely Errored Frame alarm
LINE AIS	Line alarm indication signal (AIS) alarm
LINE RDI	Line remote defect indication (RDI) alarm (also known as FERF)
PATH AIS	Path AIS alarm
PATH RDI	Path RDI alarm (also known as RAI or Yellow Alarm)
PATH LOP	Path loss of pointer (LOP) alarm
VT AIS	VT AIS alarm
VT RDI	VT RDI alarm (also known as RAI or Yellow Alarm)
VT LOP	VT LOP alarm

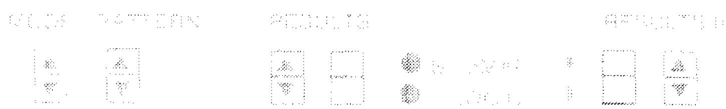
10.2.2 T-BERD 310 DS3 Transmitter Setup

1. **Set switches as follows:**

Setup	DS3
MODE	Non-channelized - M13, C-BIT, or UNFRAMED or channelized -MUXED C-BIT
PATTERN	Non-channelized - 2^23-1 or channelized - T1ESF QRSS
Channel Control	DS3-DS1
DS3 TRANSMIT TIMING	INT

2. **Press the AUX switch (LED on) and set the following auxiliary functions:**
   Select the MISC-DS3 LEVEL auxiliary function to set the DSX receive level.

MISC	**↑ transmit ↓**	**↑ receive ↓**
DS3 LEVEL	**LOW**	**DSX**



3. **Press the AUX switch (LED off) to exit the auxiliary functions**

4. **Connect the DS3 TRANSMIT jack**
   Plug a cable between this jack and the low-speed DS3 input of the SONET multiplexer or add/drop multiplexer.

10.2.3 310-1 DS1 Transmitter Setup

1. **Set switches as follows:**

MODE	T1 D4, T1 ESF, or T1
PATTERN	QRSS
TRANSMIT TIMING	INTERNAL
CODE	AMI or B8ZS

2. **Connect the DS1 TRANSMIT jack (side panel)**
   Plug a cable between this jack and the low-speed DS1 input of the SONET multiplexer or add/drop multiplexer.

10.2.4 T-BERD 310 SONET Received Signal Analysis

1. **Press the RESTART switch**
   Clear the old results and start new test.

2. **Verify the SONET Status LEDs**
   The SONET Signal Present, Frame Sync, Path PTR Pres and VT PTR Pres (if applicable) LEDs should illuminate indicating a valid framed SONET signal. For optical inputs on the 310-12 and 310-14R options, verify the side-panel LED above either OC-1/OC-3 RECEIVE or OC-12 RECEIVE optical connector illuminates when the cable is connected indicating a signal is present.

3. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected in the SONET overhead, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *SONET Results Interpretation* for additional information concerning the results. Note any SONET alarms indicated on the front panel or in the SUMMARY category as follows:

LOS	Loss of Signal alarm
LOF	Loss of Frame alarm
SEF	Severely Errored Frame alarm
LINE RDI	Line remote defect indication (RDI) alarm (also known as FERF)
PATH AIS	Path AIS alarm
PATH RDI	Path RDI alarm (also known as RAI or Yellow Alarm)
PATH LOP	Path loss of pointer (LOP) alarm
VT AIS	VT AIS alarm
VT RDI	VT RDI alarm (also known as RAI or Yellow Alarm)
VT LOP	VT LOP alarm

10.2.5 SONET Results Interpretation

The T-BERD 310 monitors the SONET signal overhead information and presents the test results in the SONET categories (SECTION, LINE, PATH, and VT) as follows:

SECTION Category

FRM WORD ERR and SON SEF SEC — Frame Word Errors and SONET Severely Errored Frame Seconds indicate incorrect framing bits are being generated by the SONET equipment or corrupted during transmission.

SECT BIP ERR and SECT EQU BER — Bit interleave parity errors indicate the data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

SONET RX FREQ — The SONET received frequency measurement verifies the received SONET signal frequency in Hertz. If the result is out of specification, it appears in the SUMMARY category.

LINE Category

POINTER JUST, POINTER INC, POINTER DEC, POINTER NDF, and POINTER DATA — Line pointer justification results monitor for excessive changes in the SPE payload pointer, which indicates a network timing problem between SONET nodes.

APS MSG CNT, APS INFO, and APS CONFIG — Automatic protection switching results indicate the number of APS messages that have been received, the last APS message received, and the APS configuration.

LINE UAS— Measures the total unavailable seconds due to excessive bit errors, loss of pointer, or AIS condition. The result appears in the SUMMARY category when an error exists.

LINE BIP ERR and LINE EQU BER — Bit interleave parity errors indicate the data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

PATH Category

PATH TRACE — The Path Trace result determines the origin of the signal and is a convenient method of determining path connectivity.

PATH UAS — Measures the total unavailable seconds due to excessive bit errors, loss of pointer, or AIS condition. The result appears in the SUMMARY category when an error exists.

PATH BIP ERR and PATH EQU BER — Bit interleave parity errors indicate the data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

VT Category

VT UAS — Measures the total unavailable seconds due to excessive bit errors, loss of pointer, or AIS condition. The result appears in the SUMMARY category when an error exists.

VT BIP ERR and VT EQU BER — Bit interleave parity errors indicate the data has been corrupted. The T-BERD 310 interprets the BIP rates and determines the actual equivalent bit error rate occurring on the live data.

VT PTR JUST, VT PTR INC, VT PTR DEC, VT PTR NDF, and VT PTR DATA — VT pointer justification results monitor for excessive changes in the VT payload pointer, which indicates a network timing problem between SONET nodes.

10.2.6 T-BERD 310 DS3 Receiver Setup and DS3 Payload Analysis

Perform the following procedure to analyze a DS3 payload dropped from a SONET signal.

1. Set switches as follows:

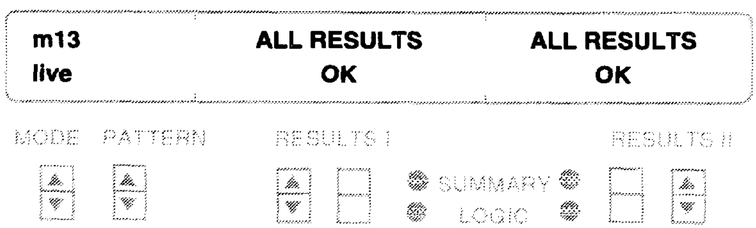
DS3 SOURCE	SONET
Setup	DS3
MODE	AUTO

NOTE: If the DS3 signal is properly framed (DS2 and DS1 framing), DS1 or E1 channels can also be dropped and monitored. The DS1 channels can be dropped to either the 310-1 DS1/DS0 Analyzer Option or DS1 DROP jack (side panel) and an external DS1 test set. The E1 channels can be dropped to the E1 DROP jack (side panel) and an external E1 test set.

2. Press the RESTART switch
Clear the old results and start new test.

3. Verify the Primary DS3 Status LEDs
These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), DS2 Frame Sync (if applicable), and Pattern Sync (if applicable).

4. Verify the framing format and pattern in the MODE/PATTERN window



5. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected in the DS3 payload, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

10.2.7 T-BERD 310 Results Interpretation

The BPV and SIGNAL category test results (except RX FREQ) are not applicable for this application since the DS3 signal is generated by the T-BERD 310. Refer to Section 3.1 for applicable in-service test results.

10.2.8 310-1 DS1 Receiver Setup and DS1 Payload Analysis

Perform the following procedure to analyze a DS1 payload dropped from a SONET signal when the T-BERD 310 indicates *ds1 asyn* or *ds1 byte* mapping.

1. **Press the DS1 SOURCE switch and select SONET DROP**

2. **Press the RESTART switch**
   Clear the old results and start a new test.

3. **Verify the 310-1 Status LEDs**
   These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync (if applicable).

4. **Verify the 310-1 RESULTS I test results**
   Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

10.2.9 310-1 Results Interpretation

When monitoring a DS1 payload from a SONET signal, observe the results in the LOGIC, FRAME, and SIGNAL categories.

NOTE: The BPV category and RX LVL dBdsx result are not applicable since the DS1 channel is dropped internally from within a SONET signal.

LOGIC Category

Logic error results — DS1 bit error rate testing (BERT) involves transmitting a DS1 test pattern from the DS1 input and dropping the same DS1 signal out of the SONET signal. The transmitted and received signals are compared. Any change in the bit patterns is counted as a bit error. Verification the test pattern is received through the SONET device also insure continuity along the entire transmission path.

FRAME Category

Frame error results — Since the DS1 framing format is a specific pattern, it can be considered a test pattern. Receiving a frame error is similar to receiving a bit error while testing with a DS1 test pattern. The frame error rate approximates the bit error rate occurring on live data. However, since frame errors make up a very small percentage of the total bits, the frame error rate gives a good representation of the bit error rate only at very high error rates or over extended test periods.
CRC error results (ESF framing only) — CRC errors indicate the integrity of the line at any error rate.

SIGNAL Category

RX FREQ — The DS1 received frequency result is pertinent to DS1 signal processing. Note that if the received frequency is out of specification (< 1,543,923 or > 1,544,077 Hz), the result automatically appears in the SUMMARY category.

TIMING SLIPS — Refer to the Timing Slips application (Section 3) to measure timing slips.

TESTING HIGH-SPEED (SONET) TO LOW-SPEED (DS3) CIRCUITS

10.3 TESTING HIGH-SPEED (SONET) TO LOW-SPEED (DS3) CIRCUITS

- Test SONET multiplexer (SM), add/drop multiplexer (ADM), or digital cross-connect system (DCS) circuit functionality from the high-speed SONET STS-1 or OC-n (n is 1, 3, or 12) side to the low-speed DS3 side while dropping and analyzing the DS3 payload from the SONET signal.

- Requires the 310-12, 310-13R and 310-13T, or 310-14R and 310-14T option.

Figure 10-3 illustrates how the T-BERD 310 connects to the SONET circuit to transmit the SONET signal with a DS3 payload and analyze the received DS3 payload. The following application is divided into three parts:

- T-BERD 310 SONET Transmitter Setup

- T-BERD 310 DS3 Transmitter Setup

- T-BERD 310 DS3 Receiver Setup and DS3 Payload Analysis

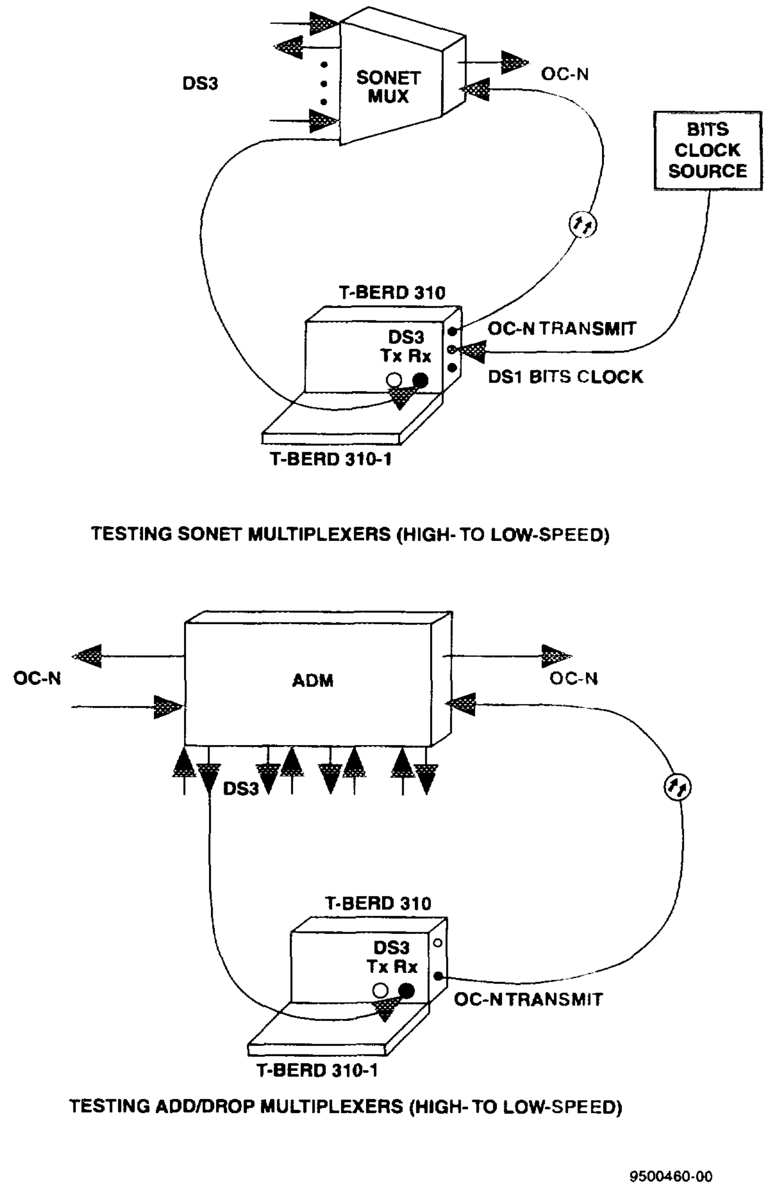


Figure 10-3
Setup for Testing High- to Low-Speed (DS3) SONET Circuits

10.3.1 T-BERD 310 SONET Transmitter Setup

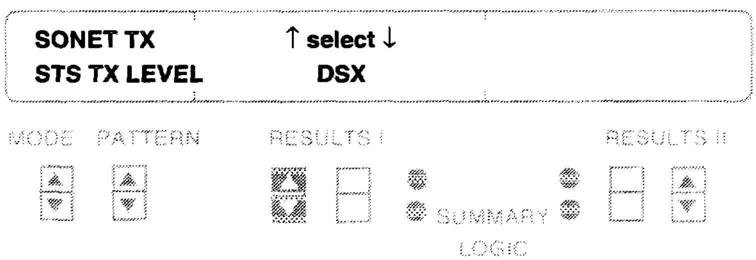
1. **Set switches as follows:**

Setup	SONET TX
RATE	STS-1, OC-1, OC-3, or OC-12
PAYLOAD	DS3 ASYN INT
Channel Control	SONET-STS
INSERT	OC-3, 1 to 3 or OC-12, 1 to 12
SONET TRANSMIT TIMING	DS1 BITS CLK or INT

NOTE: For this test, external BITS clock reference is the recommended timing source. This source can be connected by a bantam jack into the side-panel DS1 BITS CLOCK jack. If INTERNAL timing is used, pointer adjustments can be generated by the ADM due to the difference in timing of the signal from the T-BERD 310. RECOVERED timing can also be used, but only if this does not cause a timing loop (i.e., the ADM is using the line timing from the T-BERD 310).

2. **Press the AUX switch (LED on) and set the following auxiliary functions:**

   If testing an STS-1 signal, select the SONET TX-STS TX LEVEL auxiliary function and set the STS-1 signal output level.



3. **Press the AUX switch (LED off) to exit the auxiliary functions**

4. **Connect the T-BERD 310 SONET transmit to a SONET input**
   Connect a SONET cable from one of the following side-panel connections to the SONET circuit input connection:

   - STS-1 TRANSMIT
   - OC-1/OC-3 TRANSMIT
   - OC-12 TRANSMIT

   NOTE: Clean optical connections with denatured alcohol before attaching them to the T-BERD 310.

5. **Connect the external bits clock reference to the T-BERD 310**
   Connect a cable from the Bits Clock Source to the DS1 BITS CLOCK jack on the T-BERD 310.

10.3.2 T-BERD 310 DS3 Transmitter Setup

1. **Set switches as follows:**

Setup	DS3
MODE	M13, C-BIT, or UNFRAMED
PATTERN	2^23-1
DS3 TRANSMIT TIMING	INT

10.3.3 T-BERD 310 DS3 Receiver Setup and Analysis

1. **Press the DS3 SOURCE switch and select EXT**

2. **Connect the DS3 source to the T-BERD 310**
   Connect a cable from the OUT port on the equipment to the DS3 RECEIVE on the front panel of the T-BERD 310.

3. **Press the RESTART switch**
   Clear the old results and start new test.

4. **Verify the Primary DS3 Status LEDs**
   These LEDs should illuminate: Signal Present, Frame Sync, C-Bit Frame (if applicable), DS2 Frame Sync (if applicable), and Pattern Sync (if applicable).

5. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected in the DS3 payload, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *T-BERD 310 Results Interpretation* for additional information concerning the results.

10.3.4 T-BERD 310 Results Interpretation

When performing an out-of-service DS3 bit error rate test, observe the results in the LOGIC, BPV, PARITY, FRAME , and SIGNAL categories. Refer to Section 4.1 for additional information on the test results.

NOTE: If the SONET Transmit Timing LED flashes, it indicates there is a problem. Check the timing connections and setup. As a default, internal timing will be used.

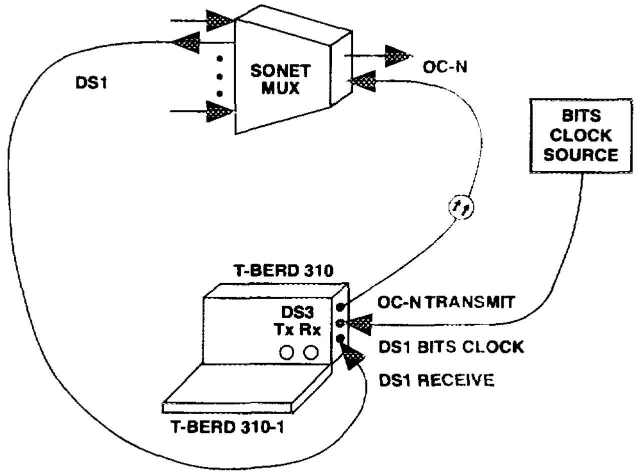
TESTING HIGH-SPEED (SONET) TO LOW-SPEED (DS1) CIRCUITS

10.4 TESTING HIGH-SPEED (SONET) TO LOW-SPEED (DS1) CIRCUITS

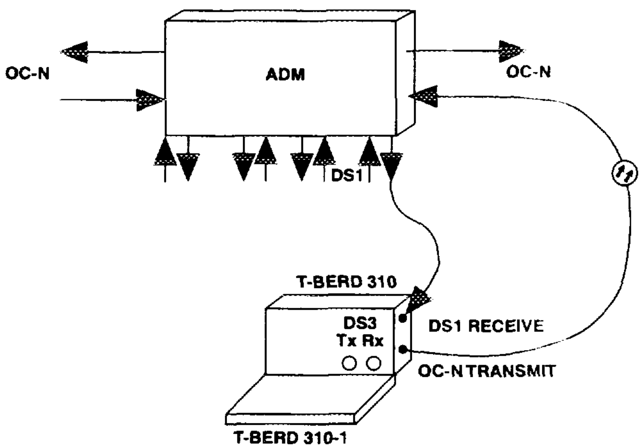
- Test SONET multiplexer (SM), add/drop multiplexer (ADM), or digital cross-connect system (DCS) circuit functionality from the high-speed SONET STS-1 or OC-n (n is 1, 3, or 12) side to the low-speed DS1 side while dropping and analyzing the DS1 payload from the SONET signal.
- Requires the 310-1 and the 310-12, 310-13R and 310-13T, or 310-14R and 310-14T option.

Figure 10-4 illustrates how the T-BERD 310 connects to the SONET circuit to transmit the SONET signal with DS1 payload and analyze the received DS1 payload. The following application is divided into three parts:

- T-BERD 310 SONET Transmitter Setup
- 310-1 DS1 Transmitter Setup
- 310-1 DS1 Receiver Setup and Analysis



TESTING SONET MULTIPLEXERS (HIGH- TO LOW-SPEED)



TESTING ADD/DROP MULTIPLEXERS (HIGH- TO LOW-SPEED)

9500727-00

Figure 10-4
Setup for Testing High- to Low-Speed (DS1) SONET Circuits

10.4.1 T-BERD 310 SONET Transmitter Setup

1. **Set switches as follows to select the STS:**

Setup	SONET TX
RATE	STS-1, OC-1, OC-3, or OC-12
PAYLOAD	DS1 ASYN INT
Channel Control	SONET-STS
INSERT	STS ID 1 to 3 (OC-3) or 1 to 12 (OC-12)

2. **Set switches as follows to select the VT:**

Channel Control	SONET-VT
INSERT	DS1 - 1 to 28 or ALL, or GP/VT - 1,1 to 7,4 or ALL

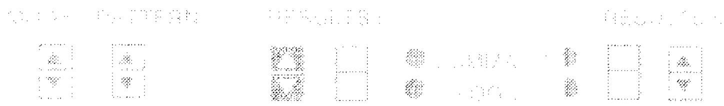
3. **Set the SONET TRANSMIT TIMING switch to DS1 BITS CLK**

NOTES: For this test, external BITS clock reference is the recommended timing source. This source can be connected to the side-panel DS1 BITS CLK jack. If INTERNAL timing is used, pointer adjustments can be generated by the ADM due to the difference in timing of the signals. RECOVERED timing can also be used, but only if this does not cause a timing loop (i.e., the ADM is using the line timing from the T-BERD 310).

If the SONET Transmit Timing LED flashes, it indicates there is a problem. Check the timing connections and setup. As a default, internal timing will be used.

4. **Press the AUX switch (LED on) and set the following auxiliary functions:**
   If testing an STS-1 signal, select the SONET TX-STS TX LEVEL auxiliary function and set the STS-1 signal output level.

SONET TX	**↑ select ↓**
STS TX LEVEL	**DSX**



5. **Press the AUX switch (LED off) to exit the auxiliary functions**

6. **Connect the T-BERD 310 SONET transmit to a SONET input**
   Connect a SONET cable from one of the following output connections to the SONET circuit input connection:

   - STS-1 TRANSMIT
   - OC-1/OC-3 TRANSMIT
   - OC-12 TRANSMIT

   NOTE: Clean optical connections with denatured alcohol before attaching them to the T-BERD 310.

7. **Connect the external bits clock reference to the T-BERD 310**
   Connect a cable from the Bits Clock Source to the DS1 BITS CLOCK jack on the T-BERD 310.

10.4.2 310-1 DS1 Transmitter Setup

1. **Set switches as follows:**

MODE	T1 D4, T1 ESF, or T1
PATTERN	QRSS
TRANSMIT TIMING	INTERNAL

10.4.3 310-1 DS1 Receiver Setup and Analysis

1. **Press the DS1 SOURCE switch and select EXT INPUT**

2. **Connect a DS1 source to the T-BERD 310**
   Connect a DS1 cable to the 310-1 side-panel DS1 RECEIVE jack.

3. **310-1 Press the RESTART switch**
   Clear the old results and start a new test.

3. **Observe the 310-1 Status LEDs**
   These LEDs should illuminate: T1 Pulses, Frame Sync, and Pattern Sync (if applicable).

4. **Verify the RESULTS I test results**
   Select the SUMMARY category. If no errors are detected, the message *ALL RESULTS OK* appears. If errors are detected, scroll through the SUMMARY category for additional errors or each category as required. Refer to *310-1 Results Interpretation* for additional information concerning the results.

10.4.4 310-1 Results Interpretation

When performing an out-of-service DS1 bit error rate test, observe the results in the LOGIC, BPV, FRAME, and SIGNAL categories. Refer to Section 4.2 for additional information on the test results.

OPTICAL
MEDIA

TESTING OPTICAL RETURN LOSS

Connection to the Circuit

T-BERD 310 Mainframe Setup

OPTICAL MEDIA TESTING

11.1 TESTING OPTICAL RETURN LOSS

- System Optical Return Loss (ORL) indicates the total amount of reflections in the system, due to connectors, splices, or fiber optic anomalies.
- This test requires the 310-16 Optical Media Test Option.

Figure 11-1 illustrates how the T-BERD 310 connects to the SONET circuit to measure the SONET signal return loss.

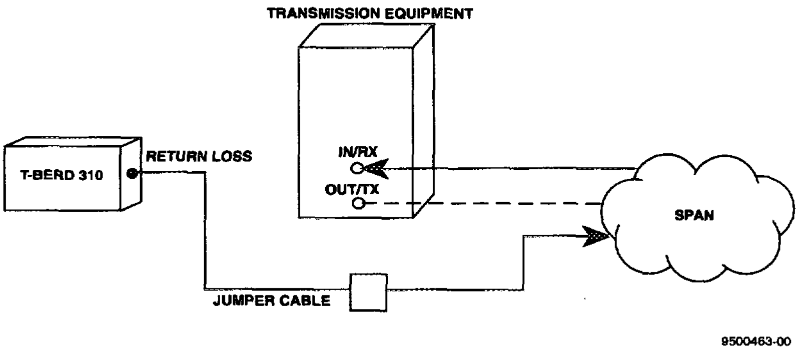


Figure 11-1
Optical Return Loss Test Connections

11.1.1 Connection to the Circuit

1. Clean fiber connectors

Clean the fiber connectors to obtain an accurate measurement.

2. Connect the RETURN LOSS/SOURCE connector

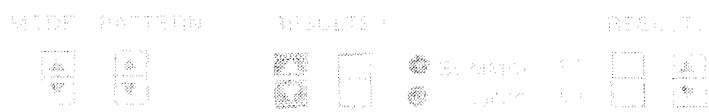
Connect the fiber optic cable to be attached to the Network Equipment Transmitter to the side-panel RETURN LOSS/ SOURCE connector. Use a jumper cable and barrel connectors if necessary.

11.1.2 T-BERD 310 Mainframe Setup

3. Press the AUX switch (LED on) and set the following auxiliary functions:

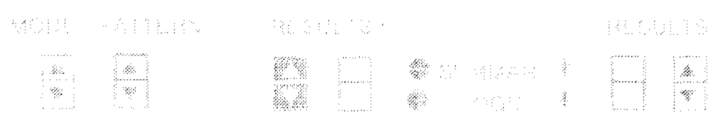
a. Select the OPTICAL TEST-RETURN LOSS auxiliary function and set to the ABSOLUTE return loss function.

OPTICAL TEST	**↑ select ↓**
RETURN LOSS	**ABSOLUTE**



b. Select the OPTICAL TEST-STABLE SOURCE auxiliary function and set the wavelength to either 1310 or 1550, depending on the system under test.

OPTICAL TEST	**↑ select ↓**
STABLE SOURCE	**1310**



4. **Press the AUX switch (LED off) to exit the auxiliary functions**

5. **Verify the RESULTS I test results**
   Select the SIGNAL category and the RETURN LOSS test result. Wait a few moments, then compare the RETURN LOSS measurement to Table 11-1.

Table 11-1
Worst-Case System Optical Return Loss Values for Single-Longitudinal Mode (SLM) Lasers

Data Rate	Link Type	Wavelength (nm)	ORL (dB)
51.84 Mbps (OC-1)	Intermediate Reach	1310	N/A
	Intermediate Reach	1550	N/A
	Long Reach	1310	N/A
	Long Reach	1550	≥20
155.52 Mbps (OC-3)	Intermediate Reach	1310	N/A
	Intermediate Reach	1550	N/A
	Long Reach	1310	N/A
	Long Reach	1550	≥20
622.08 Mbps (OC-12)	Intermediate Reach	1310	N/A
	Intermediate Reach	1550	≥24
	Long Reach	1310	≥20
	Long Reach	1550	≥24
1.244 Gbps (OC-24)	Intermediate Reach	1310	≥24
	Intermediate Reach	1550	≥24
	Long Reach	1310	≥24
	Long Reach	1550	≥24
2.488 Gbps (OC-48)	Intermediate Reach	1310	≥24
	Intermediate Reach	1550	≥24
	Long Reach	1310	≥24
	Long Reach	1550	≥24
9.953 Gbps (OC-192)	Long Reach	1550	≥30

NOTE: Long Reach optical interfaces are defined by output power levels between +2 dBm to -3 dBm and Intermediate Reach optical interfaces are defined by output power levels between -8 to -12 dBm.

TESTING INSERTION LOSS

11.2 TESTING INSERTION LOSS

- Insertion loss is a measurement that indicates the total power lost due to connectors, splices, or fiber optic anomalies.
- Requires the 310-16 Optical Media Test Option.

Figure 11-2 illustrates how the T-BERD 310 connects to the SONET circuit to measure the SONET signal power loss.

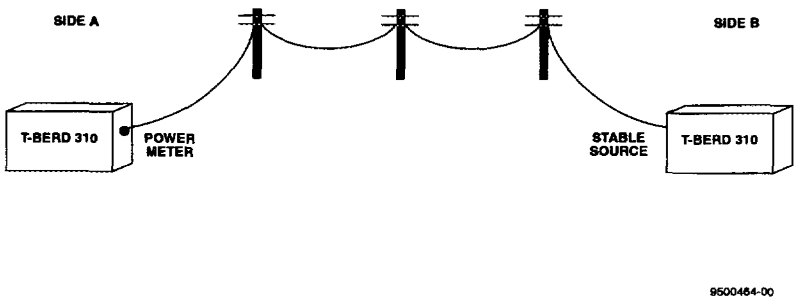


Figure 11-2
Power Loss Test Connections

11.2.1 Connection to the Circuit

1. **Clean fiber connectors**
   Clean the fiber connectors at both ends of the span to obtain an accurate measurement.

2. **Connect the POWER METER connector**
   Connect side A of the fiber optic cable to the POWER METER connector.

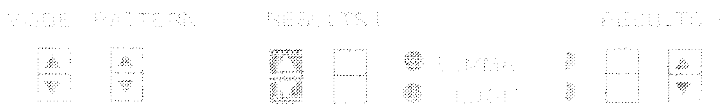
3. **Connect the RETURN LOSS/SOURCE connector**
   Connect side B of the fiber optic cable to the RETURN LOSS/ SOURCE connector.

11.2.2 T-BERD 310 Mainframe Setup, Side A

4. Press the AUX switch (LED on) and set the following auxiliary functions:

Select the OPTICAL TEST-OPTICAL PWR auxiliary function and a wavelength of either 1310 or 1550, depending on the wavelength being tested.

```
OPTICAL TEST      ↑ wavelen ↓
OPTICAL PWR         1310 nm
```



5. Press the AUX switch (LED off) to exit the auxiliary functions

6. Set the RESULTS I test results

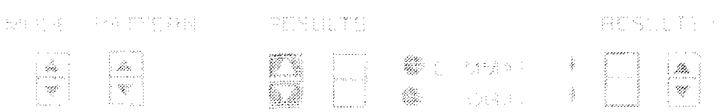
Select the SIGNAL category and the OPTICAL PWR test result.

11.2.3 T-BERD 310 Mainframe Setup, Side B

7. Press the AUX switch (LED on) and set the following auxiliary functions:

Select the OPTICAL TEST-STABLE SOURCE auxiliary function and a wavelength of either 1310 or 1550, depending on the wavelength being tested at side A and enable the transmit laser.

```
OPTICAL TEST      ↑ select ↓
STABLE SOURCE       1310
```



8. Press the AUX switch (LED off) to exit the auxiliary functions

11.2.4 T-BERD 310 Mainframe Setup, Side A

9. Verify the RESULTS I test results

Wait a few moments, then measure the OPTICAL PWR result at side A and subtract -10 dBm to eliminate the output power from side B. The absolute value of the result is the total insertion loss. For example, if OPTICAL PWR is -34.5 dBm, the total insertion loss would be -24.5 dB. Perform the test in both directions for each wavelength to obtain an average loss measurement for both wavelengths. Compare the averages with Table 11-2, or the known design loss budget to ensure the system attenuation is acceptable for the desired data rate and wavelength.

Table 11-2
Worst-Case Loss Values for
Single-Longitudinal Mode (SLM) Lasers

Data Rate	Link Type	Wavelength (nm)	Loss (dB)
51.84 Mbps (OC-1)	Intermediate Reach	1310, 1550	0-12
	Long Reach	1310, 1550	10-28
155.52 Mbps (OC-3)	Intermediate Reach	1310, 1550	0-12
	Long Reach	1310, 1550	10-28
622.08 Mbps (OC-12)	Intermediate Reach	1310, 1550	0-12
	Long Reach	1310, 1550	10-24
1.244 Gbps (OC-24)	Intermediate Reach	1310, 1550	0-12
	Long Reach	1310, 1550	10-20
2.488 Gbps (OC-48)	Intermediate Reach	1310, 1550	0-12
	Long Reach	1310, 1550	10-20

TESTING OPTICAL POWER

Connection to the Circuit

T-BERD 310 Mainframe Setup

11.3 TESTING OPTICAL POWER

- Optical Power measurement indicates the level of optical power generated by an optical laser transmitter.
- This test requires the 310-16 Optical Media Test Option.

Figure 11-3 illustrates how the T-BERD 310 connects to the SONET circuit to measure the optical power.

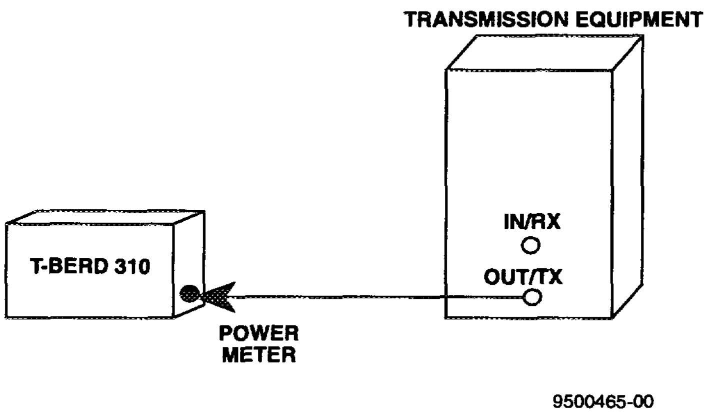


Figure 11-3
Optical Power Test Connections

11.3.1 Connection to the Circuit

1. **Clean fiber connectors**
   Clean the fiber optic jumper cable connector to obtain an accurate measurement.

2. **Connect the POWER METER connector**
   Connect the fiber optic jumper cable to the side-panel POWER METER connector.

3. **Connect the transmit laser**
   Connect the other end of the fiber to the transmit laser under test.

11.3.2 T-BERD 310 Mainframe Setup

4. **Press the AUX switch (LED on) and set the following auxiliary functions:**

   Select the OPTICAL TEST-OPTICAL PWR auxiliary function and a wavelength of either 1310 or 1550, depending on the laser wavelength being tested.

5. **Press the AUX switch (LED off) to exit the auxiliary functions**

6. **Verify the RESULTS I switch**
   Select the SIGNAL category and the OPTICAL PWR test result. Wait a few moments, then observe the OPTICAL PWR result. This indicates the total amount of transmitted power by the laser. Compare this result to the manufacturer's recommendations for the optical span configuration.

AUX
FUNCTIONS

AUXILIARY FUNCTIONS

12.1 T-BERD 310 AUXILIARY FUNCTIONS

AUX switch — Press this switch to access the auxiliary functions.

MODE switch — Press this switch to scroll through the auxiliary groups.

PATTERN switch — Press this switch to scroll through the auxiliary functions of the selected auxiliary group.

RESULTS I and RESULTS II switches — These switches are used in combination to change or enter information into the selected auxiliary function.

Group (MODE Switch)	Function (PATTERN Switch)	Description
ERR INSERT		DS3 Error Insertion Group
	LOG/BPV RT	Logic and BPV Error Insertion Rate
	FRAME ERROR	M-Frame Error Insertion Rate
	LOG/BPV BUR	Logic and BPV Error Insertion Burst Duration
ERR RECEIVE		DS3 Received Signal Error Group
	ERROR THR	Logic, BPV, and Frame Errored Second Rate Threshold
	PAT LOSS THR	Pattern Loss Threshold
	PAR ERR RT	Parity Category Error Rate Calculation
	FRM LOSS THR	Frame Synchronization Loss Threshold

Group (MODE Switch)	Function (PATTERN Switch)	Description
MUXED TX		Multiplexed Loop Code Group
	DS1 LP CODE	DS1 Loop Code Select
	PGM LPUP	Programmable Loop-Up Code
	PGM LPDN	Programmable Loop-Down Code
TIME		Time and Date Group
	SET TIME	Set Time
	SET DATE	Set Date
	TEST LENGTH	Set Test Length
	TEST TYPE	Set Test Duration Type
PRINT		Printer/Remote Control Interface Group
	INTERVAL	Timed Printout Interval
	MODE	Printout Mode
	FORMAT	Printout Format
	CUSTOM	Customized Printout Contents
	GRAPH	Print Pulse Shape Graph
	BAUD RATE	RS-232 Interface Baud Rate
	PARITY	RS-232 Interface Parity
	TERMINATOR	Printout Line Terminator
	WIDTH	Printout Line Width
	PORT	Printer/Remote Control Interface Port Selection (310-6 option)
	PRINT EVENT	Set Printout Event
	PRINT TYPE	Set Printout Type

Group (MODE Switch)	Function (PATTERN Switch)	Description
MISC		Miscellaneous Group
	USER1	User-Programmable Test Pattern
	TX X-BIT	X-Bit Transmission
	BLU SIG CRI	Blue Signal Detection Criteria
	DS1 LINECODE	DS1 Drop Output Line Coding
	BEEP CRI	Beep Criteria Coding
	PULSE MASK	Pulse Shape Mask
	FEAC ALARMS	DS3 FEAC Alarm Control
	FEAC LOOP	DS3 FEAC Message Loopback Control
	LCD CONTRAST	Display Contrast Control (310-1 option)
	DS1 SIG BITS	DS1 Signaling Transfer Mode (310-13R/T pair or 310-14R/T pair option)
	DS1 BITS CLK	DS1 Building Integrated Timing Source (BITS) Clock Termination (310-13T or 310-14T option)
	DS1/VT MAP	DS1/VT Mapping Select
	DS3 LEVEL	Set DS3 Transmit and Receive Levels
SONET RX		SONET RX Group (310-12, 310-13R, and 310-14R options)
	DS1 DROP OUT	DS1 Drop Output Source
	STS RX LEVEL	STS Receive Level
	SONET DCC	SONET Data Communication Channel Drop and Insert Control

Group (MODE Switch)	Function (PATTERN Switch)	Description
SONET TX		SONET TX Group (310-12, 310-13T, and 310-14T options)
	STS TX LEVEL	STS Transmit Level
	SONET ERR RT	SONET Error Rate Select
	SPE POINTER	Synchronous Payload Envelope Pointer Control
	PATH TRACE	Path Trace Message Insertion Control
	ORDERWIRE	Orderwire Channel Control
JITTER		DS3 Jitter Group (310-5 option)
	JIT FILTER	Jitter Bandpass Filter Select
	JIT SCALE	Jitter Amplitude Scale Select
	JIT THRESH	DS3 Jitter Threshold Select
ATM RX		ATM RX Group (310-15 option)
	NETWORK I/F	Received ATM Network Interface Select
	TEST MASK	Received ATM Cell Test Mask Control
	PROFILE Pn	Received ATM Cell Test Profile Control (n = 1 to 4)
	BW PERIOD	Received ATM Cell Test Profile Bandwidth Select
	PREVIEW	Received ATM Cell Test Profile Preview Select

Group (MODE Switch)	Function (PATTERN Switch)	Description
ATM TX		ATM TX Group (310-15 option)
	NETWORK I/F	Transmitted ATM Network Interface Select
	PROFILE Pn	Transmitted ATM Cell Test Profile Control (n = 1 to 4)
	TEST PROFILE	Transmitted ATM Cell Test Profile Select
	CELL BANDWDTH	Transmitted ATM Cell Test Profile Bandwidth Select
	PEAK BANDWDTH	Transmitted ATM Cell Test Profile Peak Bandwidth Select
	PEAK DURATION	Transmitted ATM Cell Test Profile Peak Duration Select
	HEC ERR RATE	Transmitted ATM Header Error Control Error Rate
	HEC ERR INS	Transmitted ATM Header Error Control Error Insert Control
	OAM INSERT	Transmitted ATM OAM Insert Control
	OAM FLOW	Transmitted ATM OAM Flow Control
	CORRELATION	Transmitted ATM Correlation Tag Control
OPTICAL TEST		Optical Test Group (310-16 option)
	STABLE SOURCE	Optical Source Select
	RETURN LOSS	Return Loss Measurement Type
	OPTICAL PWR	Optical Power Measurement Control

12.2 310-1 DS1/DS0 ANALYZER OPTION AUXILIARY FUNCTIONS

AUX switch — Press this switch to access the auxiliary functions.

PATTERN switch — Press this switch to scroll through the auxiliary functions.

RESULTS I and RESULTS II switches — These switches are used in combination to change or enter information into the selected auxiliary function.

Displayed Name	Description
USER1	User 1 Programmable Test Pattern
PGM LPUP	Programmable Loop-Up Code
PGM LPDN	Programmable Loop-Down Code
LP CODE	Loop Code Select
ESF LOOP[2]	ESF Loop Code Select
PRM[2]	ESF Datalink Performance Report Message Control
DATAPORT	DATAPORT Connector Output
CUSTOM	Customized Printout Format
SLIP REF[2]	DS1 Timing Slip Reference Source
SCAN TRIG	Triggered DS1 Scan Mode Evaluation Criteria
CHAN FMT[1]	FT1 Channel Format Select
CONTIG[1]	FT1 Contiguous Channel Format Select
N-CONTIG[1]	FT1 Non-Contiguous Channel Format Select

[1] Requires the 310-9B Option.
[2] Requires the 310-9B or the 310-9A Option.

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T-BERD 310 TEST RESULTS

13.1 SIGNAL STATUS LED DEFINITIONS

13.1.1 DS3 Signal Status LEDs

The Status LEDs are divided into two groups labeled PRIMARY and SECONDARY. The Primary DS3 Status LEDs (except for the SONET Present LED) refer to the signal received through the DS3 RECEIVE jack. The Primary DS3 Status LEDs also indicate the condition of the DS3 signal dropped from a SONET DS3 payload. The Secondary Status LEDs refer to the DS3 signal received through the SECONDARY DS3 RECEIVE jack when the DS1 Insert Option is installed. The Status LEDs are described as follows:

Signal Present — Illuminates when the T-BERD 310 detects valid DS3 pulses. If the received signal is lost, the LED goes out and the Signal Loss LED illuminates.

Frame Sync — Illuminates when the T-BERD 310 acquires M13 or C-bit frame synchronization. If the received framing format is lost, the LED goes out and the Frame Loss LED illuminates.

C-Bit Frame — Illuminates when the T-BERD 310 acquires C-bit frame synchronization.

Idle Present — Illuminates when the T-BERD 310 detects a DS3 Idle Signal.

DS2 Frame Sync — Illuminates when the T-BERD 310 synchronizes to the DS2 framing format corresponding to the dropped DS1 channel. The T-BERD 310 must be synchronized with the DS2 framing format before a DS1 signal can be inserted. If the received DS2 framing format is lost, the LED goes out and the DS2 Frame Loss LED illuminates.

Pattern Sync — Illuminates when the T-BERD 310 synchronizes to the test pattern displayed in the PATTERN window. If pattern synchronization is lost, the LED goes out and the Pattern Loss LED illuminates.

13.1.2 SONET Signal Status LEDs

Signal Present — SONET signal detected from the selected side-panel SONET receive jack. Subsequent loss of signal causes the Signal Present LED to go out and the Signal Loss LED illuminates.

Frame Sync — Frame synchronization acquired. Subsequent loss of frame synchronization causes the Frame Sync LED to go out and the Frame Loss LED illuminates.

Path PTR Pres — STS Path pointer present.

VT PTR Pres — Virtual tributary pointer present; indicates DS1s are embedded in the received SONET signal.

Concat Payload—Concatenated pointer value detected in the current receive STS group.

13.1.3 ATM Signal Status LEDs

Cell Sync — Cell Delineation (CD); cell synchronization acquired. Subsequent loss of cell synchronization causes the Cell Sync LED to go out and the Cell Sync Loss LED to illuminate.

ATM AIS — ATM alarm condition exists. Since the ATM AIS only illuminates when the AIS alarm is in the address specified in the receive mask, the LED extinguishes when the receive profile or cell address is changed.

ATM RDI — Remote defect indication alarm received; indicates a downstream failure (Loss of Signal, Loss of Frame, AIS, etc).

13.2 SIGNAL ALARM LED DEFINITIONS

13.2.1 DS3 Signal Alarm LEDs

The Alarm LEDs provide information about the current and historical alarm conditions related to the received DS3 signal. The Alarm LEDs are divided into two groups labeled PRIMARY and SECONDARY with two columns (current and history) each. The Primary Alarm LEDs (except for the SONET Loss LED) refer to the signal received through the DS3 RECEIVE jack. The Primary Alarm LEDs also indicate the condition of the DS3 signal dropped from a SONET DS3 payload. The Secondary Alarm LEDs refer to the signal received through the SECONDARY DS3 RECEIVE jack when the DS1 Insert Option is installed. .

HISTORY RESET switch — This switch clears all History LEDs on the T-BERD 310. This switch does not restart a test, nor does it affect any of the Alarm LEDs or accumulated results. It is not operable when the **DISPLAY HOLD** switch is activated. The **RESTART** switch also clears the History LEDs.

The Alarm LEDs (inside columns) illuminate when an alarm condition occurs and remain illuminated as long as the alarm exists. When the alarm condition is cleared, the Alarm LED goes out and its History LED (outside columns) illuminates. The History LEDs indicate past occurrences of the alarm and remain illuminated until either the **HISTORY RESET** switch is pressed or a test restart is initiated. The Primary Alarm LEDs are described as follows:

Signal Loss — Illuminates when DS3 pulses are no longer detected after initial signal detection. When the DS3 pulses are detected again, the LED goes out, and its History LED and the Signal Present LED illuminate.

Frame Loss — Illuminates when the T-BERD 310 loses DS3 frame synchronization. When DS3 framing is detected again, the LED goes out, and its History LED and the Frame Sync LED illuminate. The ERR RECEIVE-FRM LOSS THR auxiliary function sets the frame loss criteria.

DS2 Frame Loss — Illuminates when the T-BERD 310 loses frame synchronization to the DS2 signal for the corresponding dropped DS1 channel. When DS2 framing is detected again, the LED goes out, and its History LED and the DS2 Frame Sync LED illuminate.

Pattern Loss — Illuminates when the T-BERD 310 loses DS3 pattern synchronization. When the pattern is resynchronized again, the LED goes out, and its History LED and the Pattern Sync LED illuminate. The ERR RECEIVE-PAT LOSS THR auxiliary function sets the pattern loss criteria.

Blue (AIS) — Illuminates when the T-BERD 310 detects the Blue Signal (Alarm Indication Signal). When the Blue Signal is no longer detected, the LED goes out and its History LED illuminates. The MISC-BLU SIG CRI auxiliary function sets Blue Signal detection criteria.

Yellow — Illuminates when the T-BERD 310 detects the Yellow Alarm or Far-End Out-of-Frame (FEOOF) signal (X-bits set to zero). When the Yellow Alarm is no longer detected, the LED goes out and its History LED illuminates.

Far-End Alarm — Illuminates when the T-BERD 310 detects Far-End Alarm and Control (FEAC) messages in the C-bit parity framing format (third C-bit in the M1 subframe). When the Far-End Alarm is no longer detected, the LED goes out and its History LED illuminates. The alarm messages are reported in the SUMMARY category.

SONET Loss — Illuminates only when the T-BERD 310 no longer detects a valid SONET signal from either the side-panel STS-1 RECEIVE jack or OC-1/3, OC-12 RECEIVE connector of a SONET drop option. When a valid SONET signal is detected again, the LED goes out, and its History LED and the SONET Present LED illuminate.

Power Loss — Illuminates when the T-BERD 310 regains power after power was lost.

13.2.2 SONET Signal Alarm LEDs

SIGNAL LOSS — Indicates no SONET pulse signals present. When the signal is acquired again, the LED goes out, and the associated History and Signal Present LEDs illuminates.

FRAME LOSS — Indicates loss of frame synchronization. When synchronization is acquired again, the LED goes out, and the associated History and Frame Sync LEDs illuminates.

SECTION BIP — Flashes on for 100 milliseconds whenever a section Bit Interleaved Parity (BIP) error occurs. When the Section BIP LED goes out, the associated History LED illuminates until a restart or history reset occurs.

LINE AIS — Line alarm indication signal (AIS) alarm is declared after detecting a 111 pattern in the Line overhead APS byte (K2), Bits 6 to 8, for five consecutive frames. Line AIS is removed after detecting a pattern other than 111 in Bits 6-8 of byte K2 for five consecutive frames. Line AIS indicates to downstream equipment that upstream section terminating equipment (STE) has detected loss of signal or loss of framing.

LINE RDI — Line remote defect indication (RDI) alarm (also known as far-end receive fail (FERF) alarm) is declared after detecting a 110 pattern in the Line overhead APS byte (K2), Bits 6 to 8, for five consecutive frames. Line RDI is removed after detecting a pattern other than 110 in Bits 6-8 of byte K2 for five consecutive frames. Line RDI alerts an upstream device of a downstream failure, such as loss of signal, loss of frame, or Line AIS.

LINE BIP — Flashes when a line Bit Interleaved Parity (BIP) error occurs. When the Line BIP LED goes out, the associated History LED illuminates until a restart or history reset occurs.

PATH AIS — Path AIS alarm is declared after detecting an all ones pattern in the Line overhead pointer bytes (H1 and H2) for three consecutive frames. Path AIS is removed when a valid set of pointer bytes and active new data flags (NDFs) are received, or when a valid pointer value is observed in three consecutive frames. Path AIS alerts the downstream path terminating equipment (PTE) that an upstream failure has occurred.

PATH LOP — Path loss of pointer (LOP) alarm is declared when a valid pointer value cannot be determined from the Line overhead pointer bytes (H1 and H2). Specifically, Path LOP is declared if a valid pointer is not found in eight consecutive frames, if eight consecutive active NDFs are received without the corresponding concatenation indication. The Path LOP alarm is removed when a consistent pointer value or concatenation indication is received for three consecutive frames.

PATH RDI — Path RDI alarm (also known as RAI or Yellow Alarm) is declared after detecting a one in Bit 5 of the Path status byte (G1) for five consecutive frames. STS Path RDI is removed after Bit 5 of byte G1 contains a zero for five consecutive frames. Path RDI indicates to the upstream PTE that a downstream failure has been detected.

PATH BIP — Flashes on for 100 milliseconds whenever a path Bit Interleaved Parity (BIP) error occurs. When the Path BIP LED goes out, the associated History LED illuminates until a Restart or History Reset is initiated.

VT AIS — VT AIS alarm is declared after detecting an all ones pattern in the VT pointer bytes (V1 and V2) for three consecutive VT superframes. VT Path AIS is removed under two conditions: when a valid VT pointer, valid VT size, and the NDF 1001 flag are detected, or three consecutive VT superframes containing a valid VT pointer, valid VT size, and a normal NDF are detected. VT AIS alerts the downstream VT PTE of an upstream failure.

VT LOP — VT LOP alarm is declared when a valid pointer value cannot be determined from the VT Path overhead bytes (V1 and V2). Specifically, VT Path LOP is declared if a valid pointer is not found in eight consecutive frames, if eight consecutive active NDFs are received without the corresponding concatenation indication. The VT Path LOP alarm is removed when a consistent pointer value or concatenation indication is received for three consecutive frames.

VT RDI — VT RDI alarm (also known as RAI or Yellow Alarm) is declared after detecting a one in Bit 8 of the VT Path overhead byte (V5) for five consecutive VT superframes. The VT Path RDI alarm is removed when a zero is detected in Bit 8 of byte V5 for five consecutive frames. VT RDI indicates to the upstream VT PTE that a downstream failure has been detected.

VT BIP—Flashes on for 100 milliseconds whenever a virtual tributary Bit Interleaved Parity (VT BIP) error occurs. When the Line BIP LED goes out, the associated History LED illuminates and stays lit until a Restart or History Reset is initiated.

PATH PTR ADJUST —Flashes on for 100 milliseconds whenever a change in the STS path pointer value occurs. When this goes out, the associated History LED illuminates and stays lit until a Restart or History Reset is initiated.

VT PTR ADJUST — Flashes on for 100 milliseconds whenever a change in the virtual tributary (VT) path pointer value occurs. When this goes out, the associated History LED illuminates and stays lit until a Restart or History Reset is initiated.

13.2.3 ATM Signal Alarm LEDs

Cell Sync Loss — Illuminates after seven consecutive errored HECs are received and remains illuminated until six consecutive unerrored HECs are received. When this goes out, the associated History LED illuminates and stays lit until a Restart or History Reset is initiated.

ATM AIS — Illuminates after an OAM AIS cell is received in the selected receive profile, and remains illuminated until no OAM AIS cells are received for 3 consecutive seconds. When this goes out, the associated History LED illuminates until a restart or history reset occurs.

ATM RDI — Illuminates after an OAM RDI cell is received in the selected received profile, and remains illuminated until no OAM RDI cells are received for 3 consecutive seconds. When this goes out, the associated History LED illuminates until a restart or history reset occurs.

13.3 SUMMARY CATEGORY

When all SUMMARY results are error-free, the message *ALL RESULTS OK* is displayed. When an error is detected, the appropriate test result appears in the SUMMARY category window (the results are identified in the following sections). If no signal is detected, the message *ALL RESULTS UNAVAILABLE* appears in the display. When more than one error is detected, press either the **RESULTS I Results** switch or **RESULTS II Results** switch to scroll through the results.

13.3.1 DS3 Summary Test Results

The following DS3 test results appear in the SUMMARY category when they begin to detect error conditions.

- BIT ERRORS (LOGIC category)
- SLIPS (LOGIC category)
- VIOLATIONS (BPV category)
- PAR ERRORS (PARITY category)
- C-BIT ERRORS (PARITY category)
- FEBE (PARITY category)
- FRM ERRORS (FRAME category)
- DS2 FRM ERR (FRAME category)
- RX FREQ (SIGNAL category)
- FEAC Messages

13.3.2 FEAC Message and Loop Code Summary Test Results

The Far-End Alarm and Control (FEAC) messages (Table 13-1) and loop codes (Table 13-2) appear in the SUMMARY category under the FEAC Code result. The FEAC messages are accumulated as they are detected.

Only the last FEAC loop code is stored in the FEAC Code result. The results remain in the SUMMARY category until a test restart is initiated. The messages comply with the ANSI T1.107a-1990 standard and can be transmitted using the MISC-FEAC ALARMS and MISC-FEAC LOOP auxiliary functions. They are also printed as status (loop code messages) and alarm messages.

Table 13-1
Far-End Alarm and Control Messages

Message	Description
DS3 EF SA	DS3 Equipment Failure, Service Affecting (Type 1 equipment failure)
DS3 L/H	DS3 Loss-of-Signal/High Bit Error Ratio
DS3 OOF	DS3 Out-of-Frame, Loss of DS3 Frame Synchronization
DS3 AIS RX	DS3 Alarm Indication Signal Received
DS3 IDLE RX	DS3 Idle Signal Received
DS3 EF NSA	DS3 Equipment Failure, Non-Service Affecting (Type 2 equipment failure)
COMM EF NSA	Common Equipment Failure, Non-Service Affecting (Type 2 equipment failure)
MULT DS1 L/H	Multiple DS1 Loss-of-Signal/High Bit Error Ratio
DS1 EF SA	DS1 Equipment Failure, Service Affecting (Type 1 equipment failure)
SING DS1 L/H	Single DS1 Loss-of-Signal/High Bit Error Ratio
DS1 EF NSA	DS1 Equipment Failure, Non-Service Affecting (Type 2 equipment failure)

Table 13-2
FEAC Far-End Loop Code Messages

Message	Description
ALL DS1 LPDN	All DS1 Lines loop-down code
ALL DS1 LPUP	All DS1 Lines loop-up code
DS1 xx LPDN	DS1 Line No. xx loop-down code (xx = 1 to 28)
DS1 xx LPUP	DS1 Line No. xx loop-up code (xx = 1 to 28)
DS3 LN LPDN	DS3 Line loop-down code
DS3 LN LPUP	DS3 Line loop-up code

13.3.3 SONET Option Summary Test Results

The following SONET test results appear in the SUMMARY category when the T-BERD 310 has properly recognized and synchronized to a SONET signal:

- APS MSG CNT — Automatic Protection Switching Message Count
- FRM WORD ERR — Frame Word Errors
- LINE BIP ERR — Line BIP Errors
- LINE FEBE — Line Far-End Block Errors
- LINE UAS — Line Unavailable Seconds
- PATH BIP ERR — Path BIP Errors
- PATH FEBE — Path FEBE
- PATH UAS — Path Unavailable Seconds
- POINTER SIZE — SPE Pointer Size

- SECT BIP ERR — Section Bit Interleaved Parity Errors
- SON RX FREQ — SONET Receive Frequency
- SONET Alarms:

  SEF — Severely Errored Frame
  LOS — Loss of Signal
  LOF — Loss of Frame
  LINE AIS — Line Alarm Indication Signal
  LINE RDI — Line Remote Defect Indication
  PATH AIS — Path AIS
  PATH RDI — Path RDI
  PATH LOP — Path Loss Of Pointer
  VT AIS — VT AIS
  VT RDI — VT RDI
  VT LOP — VT LOP

- VT BIP ERR — VT BIP Errors
- VT FEBE — VT FEBE
- VT UAS — VT Unavailable Seconds

13.3.4 OC-3c ATM Option Summary Test Results

When the OC-3c ATM Option is installed, the SUMMARY category automatically displays the ATM alarms when they exceed predefined conditions. The ATM Alarm test result displays current (C) and historical (H) signal status for the following conditions (nn = C, H, or HC):

- ATM AIS nn — ATM Alarm Indication Signal
- ATM RDI nn — ATM Remote Defect Indication
- OUT OF SYNC nn — Out of Synchronization
- SYNC LOSS nn — Loss of Synchronization
- SYNC FAIL nn — Synchronization Failure

13.3.5 DS3 Jitter Option Summary Test Results

When the DS3 Jitter Option is installed and the JITTER-JIT THRESH auxiliary function threshold is set, the SUMMARY category automatically displays the MAX WB JIT and MAX HB JIT test results when the threshold is exceeded.

13.4 LOGIC CATEGORY

13.4.1 DS3 Test Results

BIT ERRORS

Bit Errors — The number of received pattern bits which have a value opposite that of the corresponding transmitted bit pattern since initial DS3 pattern synchronization. The result also appears in the SUMMARY category (count > 0). The MISC-BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

BIT ERR RT

Bit Error Rate— The ratio of pattern bit errors to received pattern bits over the previous block of 10^8 bits.

AV BIT ERT

Average Bit Error Rate — The ratio of pattern bit errors to the total number of received pattern bits while DS3 pattern synchronization is present.

BIT ERR SEC

Bit Errored Seconds — The number of seconds during which one or more pattern bit errors occurred since initial DS3 pattern synchronization.

BIT %EFS

Bit, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no pattern bit errors were detected, to the total number of seconds while DS3 pattern synchronization is present.

BIT THR ES

Bit, Threshold Errored Seconds — The number of seconds during which the pattern bit error rate exceeded or equaled the user-defined threshold. The threshold is set through the ERR RECEIVE-ERROR THR auxiliary function. The MISC-BEEP CRI auxiliary function (THR ERR SEC) can be enabled to beep when the threshold is exceeded.

SYNC ES

Synchronous Errored Seconds — The number of seconds during which at least one pattern bit error has occurred. Each second is initiated by, and synchronized to, a pattern bit error.

SYNC L SEC

Synchronization Loss Seconds — The number of seconds during which the receiver has lost pattern synchronization, even momentarily, since initial DS3 pattern synchronization.

SLIPS

Slips — The number of times the received pattern becomes skewed relative to the expected (i.e., internally generated) test pattern. When a slip is detected, the T-BERD 310 automatically resynchronizes to the received pattern. However, pattern bit errors are not suppressed during this process. Pattern slips are available only when using pseudorandom patterns. The result also appears in the SUMMARY category (count > 0).

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AVAIL SEC

Available Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is less than 10^{-3}.

%AVAIL SEC

% Available Seconds — The ratio, expressed as a percentage, of available seconds to the total elapsed seconds since pattern synchronization.

SEV ERR SEC

Severely Errored Seconds — A count of seconds during which the bit error rate is worse than 10^{-3} within the available time.

%SEVERR SEC

% Severely Errored Seconds — The ratio, expressed as a percentage, of severely errored seconds to the number of available seconds.

CSES

Consecutive Severely Errored Seconds — A count of three or more contiguous severely errored seconds in which a bit error rate is worse than 10^{-3} in each second.

DEG MIN

Degraded Minutes — A count of minutes during which the bit error ratio is worse than 10^{-6} and less than 10^{-3}.

%DEG MIN

% Degraded Minutes — The ratio, expressed as a percentage, of degraded minutes to the number of available non-severely errored minutes.

UNAVAIL SEC

Unavailable Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is greater than or equal to 10^{-3}.

13.5 BPV CATEGORY

VIOLATIONS

Bipolar Violations — The number of bipolar violations (BPVs) detected since the beginning of the test. Intentional B3ZS code violations are excluded from the count. The result also appears in the SUMMARY category (count > 0) and the Secondary DS3 category results. The MISC-BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

BPV ERR RT

BPV Error Rate — The ratio of BPVs to received bits over the previous block of 10^8 bits.

AV BPV ERT

Average BPV Error Rate—The ratio of BPVs to the total number of received bits since the beginning of the test.

BPV ERR SEC

BPV Errored Seconds — The number of seconds during which one or more BPVs occurred since the beginning of the test.

BPV %EFS

BPV, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no BPVs were detected, to the total number of seconds since the beginning of the test.

BPV THR ES

BPV Threshold Errored Seconds — The number of seconds during which the BPV rate exceeded or equaled the user-defined threshold. The threshold is set through the ERR RECEIVE-ERROR THR auxiliary function. The MISC-BEEP CRI auxiliary function (THR ERR SEC) can be enabled to beep when the threshold is exceeded.

13.6 PARITY CATEGORY

PAR ERRORS

Parity (P-bit) Errors — The number of parity errors detected since initial DS3 frame synchronization. The result also appears in the SUMMARY category (count > 0) and the Secondary DS3 category results. The MISC-BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

PAR ERR RT

Parity (P-bit) Error Rate — The ratio of parity errors to (1) the number of bits over which parity was calculated (Bit mode), or (2) the number of DS3 M-frames received (Block mode). The error rate is computed over the previous block of 10^8 bits. The result is derived as a bit or block error rate based on the setting of ERR RECEIVE-PAR ERR RT auxiliary function.

AV PAR ERT

Average Parity (P-bit) Error Rate — The ratio of parity errors to (1) the number of bits over which parity was calculated (Bit mode), or (2) the number of DS3 M-frames received (Block mode). The error rate is computed while DS3 frame synchronization is present. The result is derived as a bit or block error rate based on the setting of the ERR RECEIVE-PAR ERR RT auxiliary function.

PAR ERR SEC

Parity (P-bit) Errored Seconds — The number of seconds during which one or more parity errors occurred since initial DS3 frame synchronization.

PAR %EFS

Parity (P-bit), Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no parity errors were detected, to the total number of seconds while DS3 frame synchronization is present.

C-BIT ERRORS

C-bit Parity Errors — The number of parity errors detected since initial DS3 C-bit frame synchronization. The result also appears in the SUMMARY category (count > 0) and the Secondary DS3 category results. The MISC-BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

C-BIT ERR RT

C-bit Parity Error Rate — The ratio of C-bit parity errors to (1) the number of bits over which C-bit parity was calculated (Bit mode), or (2) the number of DS3 C-bit M-frames received (Block mode). The error rate is computed over the previous block of 10^8 bits. The result is derived as a bit or block error rate based on the setting of the ERR RECEIVE-PAR ERR RT auxiliary function.

AV C-BIT ERT

Average C-bit Parity Error Rate — The ratio of C-bit parity errors to (1) the number of bits over which C-bit parity was calculated (Bit mode), or (2) the number of DS3 C-bit M-frames received (Block mode). The error rate is computed while DS3 C-bit frame synchronization is present. The result is derived as a bit or block error rate based on the setting of the ERR RECEIVE-PAR ERR RT auxiliary function.

C-BIT TYPE A

C-bit Parity Errored Seconds, Type A — The number of seconds during which one and only one C-bit parity error occurred since initial DS3 C-bit frame synchronization.

C-BIT TYPE B

C-bit Parity Errored Seconds, Type B — The number of seconds during which 2 to 44 C-bit parity errors occurred since initial DS3 C-bit frame synchronization.

C-BIT TYPE C

C-bit Parity Errored Seconds, Type C — The number of seconds during which more than 44 C-bit parity errors occurred since initial DS3 C-bit frame synchronization.

C-BIT %EFS

C-bit Parity, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no C-bit parity errors were detected, to the total number of seconds while DS3 C-bit frame synchronization is present.

FEBE

Far-End Block Errors — The number of far-end block errors (FEBEs) detected since initial DS3 C-bit frame synchronization. The result also appears in the SUMMARY category (count > 0) and the Secondary DS3 category results. The MISC-BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

FEBE RT

Far-End Block Error Rate — The ratio of FEBEs to (1) the number of bits over which C-bit parity was calculated (Bit mode), or (2) the number of DS3 C-bit M-frames received (Block mode). The error rate is computed over the previous block of 10^8 bits. The result is derived as a bit or block error rate based on the setting of the ERR RECEIVE-PAR ERR RT auxiliary function.

AV FEBE RT

Average Far-End Block Error Rate — The ratio of FEBEs to (1) the number of bits over which C-bit parity was calculated (Bit mode), or (2) the number of DS3 C-bit M-frames received (Block mode). The error rate is computed while DS3 C-bit frame synchronization is present. The result is derived as a bit or block error rate based on the setting of the ERR RECEIVE-PAR ERR RT auxiliary function.

FEBE TYPE A

Far-End Block Errored Seconds, Type A — The number of seconds during which one and only one FEBE occurred since initial DS3 C-bit frame synchronization.

FEBE TYPE B

Far-End Block Errored Seconds, Type B — The number of seconds during which 2 to 44 FEBEs occurred since initial DS3 C-bit frame synchronization.

FEBE TYPE C

Far-End Errored Seconds, Type C — The number of seconds during which more than 44 FEBEs occurred since initial DS3 C-bit frame synchronization.

FEBE %EFS

Far-End Block Error, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no FEBEs were detected, to the total number of seconds while DS3 C-bit frame synchronization is present.

13.7 FRAME CATEGORY

FRM ERRORS

Frame Errors — The number of frame errors detected since initial DS3 frame synchronization. The result also appears in the SUMMARY category (count > 0) and the Secondary DS3 category results. The MISC-BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

FRM ERR RT

Frame Error Rate — The ratio of frame errors to received framing bits over the previous block of 10^8 bits.

AV FRM ERT

Average Frame Error Rate — The ratio of frame errors to the total number of received framing bits while DS3 frame synchronization is present.

FRM ERR SEC

Frame Errored Seconds — The number of seconds during which one or more frame errors occurred since initial DS3 frame synchronization.

FRM %EFS

Frame, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no frame errors were detected, to the total number of seconds while DS3 frame synchronization is present.

FRM THR ES

Frame Threshold Errored Seconds — The number of seconds during which the frame error rate exceeded or equaled the user-defined threshold. The threshold is set through the ERR RECEIVE-ERROR THR auxiliary function. The MISC-BEEP CRI auxiliary function (THR ERR SEC) can be enabled to beep when the threshold is exceeded.

FRM LOSS CNT

DS3 Frame Loss Count — The number of DS3 frame losses occurring after initial frame synchronization.

FEOOF SEC

Far-End Out-of-Frame Seconds — The number of seconds during which the received X-bits are zero within the one second interval.

NEOOF SEC

Near-End Out-of-Frame Seconds — The number of seconds during which an out-of-frame condition or an AIS (Alarm Indication Signal) is detected.

DS2 FRM ERR

DS2 Frame Errors — The number of DS2 frame errors detected since initial DS2 frame synchronization. The result applies only to the DS2 signal which contains the DS1 (or E1) channel being dropped. The count is reset when the selected dropped channel is changed such the new channel being dropped corresponds to a different DS2 signal. The result also appears in the SUMMARY category (count > 0). The MISC-BEEP CRI auxiliary function (ERROR EVENT) can be enabled to beep when the threshold is exceeded.

DS2 FRM ERT

DS2 Frame Error Rate — The ratio of detected DS2 frame errors to the total DS2 framing bits received. The result applies only to the DS2 signal that contains the DS1 channel being dropped. The count is reset when the selected dropped DS1 channel is changed such the new channel being dropped corresponds to a different DS2 signal.

DS2 AV F ERT

DS2 Average Frame Error Rate — The ratio of DS2 frame errors to the total number of received framing bits while DS2 frame synchronization is present.

TX X-BIT

Transmitted X-bit — The current setting of the transmitted X-bits when in a framed mode. The transmitted X-bits are set through the MISC-TX X-BIT auxiliary function.

RX X-BIT

Received X-bit — The current status of the received X-bits when in a framed mode. The result is available after receiving DS3 frame synchronization.

13.8 SIGNAL CATEGORY

13.8.1 DS3 Test Results

SIG L SEC

Signal Loss Seconds — The number of seconds during which the received DS3 signal was lost for all or part of a second since initial signal detection.

TX FREQ

Transmit Frequency — The frequency of the transmit clock measured in Hz.

RX FREQ

Receive Frequency — The frequency of the clock recovered from the received data measured in Hz. The result also appears in the SUMMARY category if it is out of range.

POWER

Receive Signal Power — The power level of the received DS3 signal measured in dBm.

LEVEL

Receive Signal Level — The level of the received DS3 signal in volts peak.

PULSE SHAPE

Pulse Shape — A PASS/FAIL result which shows whether the DS3 pulse shape is within the boundary of the specified pulse mask. The pulse shape mask is set through the MISC-PULSE MASK auxiliary function.

PULSE WIDTH

Pulse Width — The pulse width of the DS3 pulse measured in nanoseconds.

RISE TIME

Pulse Rise Time — The time interval between the 10% and 90% points of the rising edge of the DS3 pulse measured in nanoseconds.

FALL TIME

Pulse Fall Time — The time interval between the 10% and 90% points of the falling edge of the DS3 pulse measured in nanoseconds.

13.8.2 DS3 Jitter Option Test Results

WB JITTER

Wideband Jitter — The current wideband (10 Hz to 400 kHz) jitter amplitude, expressed in peak-to-peak UIs. This result is only available in the jitter AUTO and WIDEBAND filter modes.

MAX WB JIT

Maximum Wideband Jitter — The maximum peak-to-peak wideband jitter amplitude, expressed in peak-to-peak UIs, since initial signal presence or test restart. This result is only available in the jitter AUTO and WIDEBAND filter modes. This result is unavailable if the WB JITTER result has been out of range since test restart. If the WB JITTER result is available and then goes *OUT OF RANGE*, this result also goes *OUT OF RANGE* indicating the peak jitter reading is outside the current range.

HB JITTER

Highband Jitter — The current highband (30 kHz to 400 kHz) jitter amplitude, expressed in peak-to-peak UIs. This result is only available in the jitter AUTO and HIGHBAND filter modes.

MAX HB JIT

Maximum Highband Jitter — The maximum peak-to-peak highband jitter amplitude, expressed in peak-to-peak UIs, since initial signal presence or test restart. This result is only available in the jitter AUTO and HIGHBAND filter modes. This result is unavailable if the HB JITTER result has been out of range since test restart. If the HB JITTER result is available and then goes *OUT OF RANGE*, this result also goes *OUT OF RANGE* indicating the peak jitter reading is outside the current range.

13.8.3 Optical Media Test Option Test Results

OPTICAL PWR

Optical Power—Measures optical power at the POWER METER connector. Set the wavelength with the OPTICAL TEST-OPTICAL PWR auxiliary function. If no signal is attached, the result indicates *NO SIGNAL* in Revision G software.

RETURN LOSS

Optical Return Loss — Measures optical return loss at the RETURN LOSS/SOURCE connector. Set the type of measurement performed with the OPTICAL TEST-RETURN LOSS auxiliary function. Select the wavelength and enable the laser with the OPTICAL TEST-STABLE SOURCE auxiliary function. This result is not applicable unless the laser source is activated.

13.9 TIME CATEGORY

TIME

Current Time of Day — The current time of day in hours, minutes, and seconds. The time is set through the TIME-SET TIME auxiliary function.

DATE

Current Date — The current day and month. The date is set through the TIME-SET DATE auxiliary function.

ELAPSED TIME

Elapsed Time — The elapsed time in hours, minutes, and seconds since the last test restart. If no DS3 signal is present after test restart, the test does not begin.

TEST LENGTH

Timed Test Length — The currently set test length for a timed test in hours and minutes. The test length is set through the TIME-TEST LENGTH auxiliary function. This result is N/A unless the **TIME-TEST** auxiliary function is set to TIMED.

TIME LEFT

Timed Test Time Left — The time remaining for a timed test in hours, minutes, and seconds. This result is N/A unless the **TIME-TEST** auxiliary function is set to TIMED.

13.10 SONET SECTION CATEGORY

FRM WORD ERR

Frame Word Errors — Counts the number of errored frame alignment signal (FAS) subsets (subset of bytes A1 and A2) received since gaining initial frame synchronization.

SON SEF SEC

SONET Severely Errored Frame Seconds — Counts the number of seconds in which one or more loss of frame (LOF) alarms have occurred since gaining initial frame synchronization. A severely errored frame (SEF) is defined as four consecutive STS-N frames received with errored frame words. An LOF is defined as SEFs persisting for 3 ms or a random unframed signal for 625 microseconds.

SON LOS SEC

SONET Loss of Signal Seconds — Counts the number of seconds in which one or more SONET loss of signal (LOS) events occur. An LOS is defined as an all zeros pattern which lasts for least 100 microseconds. An LOS is removed after two consecutive valid frame alignment signals are detected without an intervening loss of signal.

SON RX FREQ

SONET Receive Frequency — Displays the recovered clock frequency of the received SONET signal in hertz.

SON TX FREQ

SONET Transmit Frequency — Displays the frequency of the transmitted SONET signal in hertz.

SECT BIP ERR

Section BIP Errors — Counts the number of times the Section BIP byte (B1) indicates an error in the previous frame since test restart. Up to eight section BIP errors can be counted in a single frame.

SECT EQU BER

Section Equivalent Bit Error Rate — Presents an equivalent Section bit error rate (BER) which is derived from the received section BIP error count since initial SONET frame synchronization.

SECT BIP ES

Section BIP Errored Seconds — Counts the number of seconds in which one or more Section BIP errors occurred since test restart. The errored second interval is not synchronous to the occurrence of the BIP error.

SECT BIP ESA

Section BIP Errored Seconds, Type A — Counts the number of seconds in which exactly one Section BIP error occurred, and no LOF or LOS alarms occurred.

SECT BIP ESB

Section BIP Errored Seconds, Type B — Counts the number of seconds in which more than one but less than 2500 Section BIP errors occurred for an STS-1, OC-1, or OC-3 signal; or less than 8800 occurred for an OC-12 signal.

SECT BIP SES

Section BIP Severely Errored Seconds — Counts the number of seconds in which more than 2500 Section BIP errors occurred for an STS-1, OC-1, or OC-3 signal; or more than 8800 occurred for an OC-12 signal.

SYNC MSG

Z1 Byte Synchronization Message — Displays the Z1 byte message after SONET frame synchronization and signal presence are detected. The test result displays the following Z1 byte messages:

20 PPM CLK — A 20 parts per million based clock is being used.
RESERVED — The received Z1 byte is reserved for other purposes.
STRATUM 1 — A Stratum 1 based clock is being used.
STRATUM 2 — A Stratum 2 based clock is being used.
STRATUM 3 — A Stratum 3 based clock is being used.
TRACE UNKN — Traceability is unknown.
UNKNOWN — Any byte other than the above.
DO NOT USE — The timing source should not be used for synchronization, as it would cause a timing loop.

13.11 SONET LINE CATEGORY

LINE BIP ERR

Line BIP Errors — Counts the number of times in which the Line BIP byte (B2) indicates an error in the previous frame since initial SONET frame synchronization. Up to eight Line BIP errors can be counted in a single frame.

LINE EQU BER

Line Equivalent Bit Error Rate — Presents an equivalent Line BER which is derived from the received Line BIP error count since initial SONET frame synchronization.

LINE BIP ES

Line BIP Errored Seconds — Counts the number of seconds in which one or more Line BIP errors occurred since initial SONET frame synchronization. The errored second interval is not synchronous to the occurrence of the BIP error.

LINE BIP ESA

Line BIP Errored Seconds, Type A — Counts the number of seconds in which exactly one Line BIP error occurred, and no LOF or LOS alarms occurred.

LINE BIP ESB

Line BIP Errored Seconds, Type B — Counts the number of seconds in which more than one but less than 2500 Line BIP errors occurred for an STS-1, OC-1, or OC-3 signal; or less than 10,000 errors occurred for an OC-12 signal.

LINE BIP SES

Line BIP Severely Errored Seconds — Counts the number of seconds in which more than 2500 Line BIP errors occurred in 1 second for an STS-1, OC-1, or OC-3 signal; or more than 10,000 errors occurred for an OC-12 signal.

LINE UAS

Line Unavailable Seconds — Counts the number of seconds in which the line is not available based on counts of consecutive line severely errored seconds, or the presence of an AIS alarm.

LINE AIS SEC

Line AIS Seconds — Counts the number of seconds in which one or more line AIS alarms occurred.

LINE FEBE

Line FEBE—Counts the line FEBEs detected. Line far-end block errors are defined in the Z2 byte for the STS-1. OC-3, and an OC-12 signal.

LINE FEBE RT

Line FEBE Rate—Presents an equivalent BER based on received line FEBE counts.

POINTER JUST

Pointer Justifications — Counts the number of times the synchronous payload envelope (SPE) pointer changed since initial SONET frame synchronization.

POINTER INC

Pointer Increments — Counts the number of times the pointer bytes (H1 and H2) indicated an increment to the path payload pointer since initial SONET frame synchronization.

POINTER DEC

Pointer Decrements — Counts the number of times the pointer bytes (H1 and H2) indicated a decrement to the path payload pointer since initial SONET frame synchronization.

POINTER NDF

Pointer New Data Flags — Counts the number of times the pointer bytes (H1 and H2) indicated an active new data flag (arbitrary change in pointer) since initial SONET frame synchronization. An active NDF occurs during a change in payload content, or after an AIS or some other failure condition. If a change in the pointer is detected for three consecutive frames, the change is counted as an NDF, even if the pointer never has an active NDF.

POINTER DATA

Pointer Data— Presents the current STS path pointer value from 0 to 782. *UNAVAILABLE* appears under a number of error conditions, such as line AIS, etc. *OUT OF RANGE* appears if the pointer value is outside 0 to 782.

POINTER SIZE

Pointer Size Bits— Indicates the binary setting of the size bits in the SONET H1 byte. The normal setting for the pointer size bits is 00 to indicate a SONET payload. If the received bits are other than 00, the result appears in the SUMMARY category.

APS MSG CNT

APS Message Count— Counts the number of transitions occurring in the switch priority field of the line overhead byte (K1), Bits 1 to 4. This is an indication of protection switch activity; it is not a direct count of protection switches.

APS INFO

APS Information — Presents the current protection switch request message and channel as indicated by the line overhead byte (K1). The displayed messages are listed in Table 13-3. ## is the channel number from 0 to 15. Since the APS data bytes (K1 and K2) may change rapidly during a protection switch operation, the display may not indicate every transition.

Table 13-3
SONET APS Information Result Messages

Message	Switch Request
## LOCKOUT	Lockout of Protection
## FORCE SW	Forced Switch
## SIG FAILH	Signal Fail High-priority
## SIG FAILL	Signal Fail Low-priority
## SIG DEGRH	Signal Degrade High-priority
## SIG DEGRL	Signal Degrade Low-priority
## MANUAL SW	Manual Switch
## WTR	Wait to Restore
## EXERCISE	Exerciser
## REVERSE	Reverse Request
## NO REVERT	Do Not Revert
## NO REQ	No Request

APS CONFIG

APS Configuration — Presents the current APS configuration: 1:n verses 1+1, and bidirectional verses unidirectional. This information is obtained from the APS line overhead byte (K2). Table 13-4 lists the possible APS configuration messages. The Mode appears on the left half of the result window, and Switching appears on the right half.

Table 13-4
SONET APS Configuration Result Message

Message	Switch Request
	Mode
1:n	Provisioned for 1:n mode
1+1	Provisioned for 1+1 mode
	Switching
BIDIR	Provisioned for Bidirectional Switching
UNIDIR	Provisioned for Unidirectional Switching
AIS	Line AIS
RDI	Line RDI

13.12 SONET PATH CATEGORY

PATH BIP ERR

Path BIP Errors — Counts the number of times in which the Path BIP byte (B3) indicates an error in the previous frame since initial SONET frame synchronization. Up to eight Path BIP errors can be counted in a single frame.

PATH EQU BER

Path Equivalent Bit Error Rate — Presents an equivalent Path BER which is derived from the received Path BIP error count since initial SONET frame synchronization.

PATH BIP ES

Path BIP Errored Seconds — Counts the number of seconds in which one or more Path BIP errors occurred since initial SONET frame synchronization. The errored second interval is not synchronous to the occurrence of the BIP error.

PATH BIP ESA

Path BIP Errored Seconds, Type A — Counts the number of seconds in which exactly one Path BIP error occurred, and no LOF or LOS alarms occurred.

PATH BIP ESB

Path BIP Errored Seconds, Type B — Counts the number of seconds in which more than one but less than 2400 Path BIP errors occurred.

PATH BIP SES

Path BIP Severely Errored Seconds — Counts the number of seconds in which 2400 or more Path BIP errors occurred since initial SONET frame synchronization.

PATH UAS

Path Unavailable Seconds — Counts the number of seconds in which the line is unavailable. The path is unavailable when 10 consecutive frame word errors are received, or when a condition leading to a failure (i.e., loss of signal) occurs. If the failure was preceded by one or more consecutive frame word errors, then path unavailability starts with the frame word errors. The path becomes available again after a minimum of 10 consecutive seconds without any frame word errors, or when the failure is removed, whichever is greater. All path related results count when the path is available. When the path is unavailable, only this result counts.

PATH AIS SEC

Path AIS/LOP Seconds — Counts the number of seconds in which one or more Path AIS or LOP occurs.

PATH FEBE

Path FEBE — Counts the number of Path BIP errors detected by the downstream PTE.

PATH FEBE RT

Path FEBE Rate — Presents an equivalent BER based on received Path FEBE counts.

PATH TRACE

Path Trace Message — Displays the 64-byte path trace ASCII message which is carried in the path overhead byte (J1). The message scrolls across the results window in a ticker tape fashion, 12 characters at a time.

SIGNAL LABEL

Signal Label — Presents the payload type being carried in the current position of the current STS. The information is derived from the Path signal label (C2) and VT overhead (V5) bytes. Any C2/V5 combinations which cannot be decoded appear as *UNRECOGNIZED*. Table 13-5 lists the signal label messages. The V5 byte for VT1.5 payloads is fully decoded. For other virtual tributary sizes (VT2, VT3, and VT6), only the floating/locked indication and size are shown.

Table 13-5
SONET Signal Label Result Messages

Displayed Name	Description
DS4NA	DS4 North American (139.264 Mb/s)
ATM	Asynchronous Transfer Mode
DQDB	Distributed Queue Dual Bus (MAN)
DS1 ASYN	DS1 Asynchronous
DS1 ASYN L	DS1 Asynchronous, Locked Mode
DS1 BIT	DS1 Bit Synchronous
DS1 BIT L	DS1 Bit Synchronous, Locked Mode
DS1 BYTE	DS1 Byte Synchronous
DS1 BYTE L	DS1 Byte Synchronous, Locked Mode
DS3 ASYN	Asynchronous DS3
FDDI	Fiber Distributed Data Interface
PATH EQNS	Path Equipped Nonspecific
PATH UNEQ	Path Unequipped
SYNTRAN	Byte Observable SYNTRAN
UNKNOWN–xxx	Undecodable. xxx is the numeric value of the C2 byte.
VT1.5 EQNS L	VT1.5 Equipped Nonspecific, Locked Mode
VT1.5 EQNS	VT1.5 Equipped Nonspecific
VT1.5 UNAS L	VT1.5 Unassigned, Locked Mode
VT1.5 UNAS	VT1.5 Unassigned
VT1.5 UNEQ L	VT1.5 Unequipped, Locked Mode
VT1.5 UNEQ	VT1.5 Unequipped
VT2 L	VT2, Locked Mode
VT2	VT2
VT3 L	VT3, Locked Mode
VT3	VT3
VT6 L	VT6, Locked Mode
VT6	VT6

13.13 SONET VIRTUAL TRIBUTARY CATEGORY

VT BIP ERR

VT BIP Errors—Counts the number of times in which the VT BIP byte (V5, Bits 1 and 2) indicates an error in the received signal. A maximum of two VT BIP errors can be counted in each SONET frame.

VT EQU BER

VT Equivalent Bit Error Rate— Presents an equivalent VT BER which is derived from the received VT BIP error count since initial SONET frame synchronization.

VT BIP ES

VT BIP Errored Seconds — Counts the number of seconds in which one or more VT BIP errors, an AIS, or VT LOP occurred.

VT BIP ESA

VT BIP Errored Seconds, Type A — Counts the number of seconds in which exactly one VT BIP error occurred.

VT BIP ESB

VT BIP Errored Seconds, Type B — Counts the number of seconds in which more than one but less than 600 VT BIP errors occurred.

VT BIP SES

VT BIP Severely Errored Seconds — Counts the number of seconds in which 600 or more VT BIP errors occurred during a single second.

VT UAS

VT Unavailable Seconds — Counts the number of seconds in which the VT path is unavailable. The path is unavailable when 10 consecutive severely errored seconds are received, or when a condition leading to a failure (i.e., loss of signal) occurs. If the failure was preceded by one or more consecutive severely errored seconds, then VT path unavailability starts with the severely errored seconds. The VT path becomes available again after a minimum of 10 consecutive seconds without any severely errored seconds, or when the failure is removed, whichever is greater. All VT path related results count when the VT path is available. When the VT path is unavailable, only this result counts.

VT AIS SEC

VT AIS/LOP Seconds — Counts the number of seconds in which one or more VT AIS or LOP occurs.

VT FEBE

VT FEBE — Counts the number of VT BIP errors detected by the downstream PTE. It is calculated by summing the FEBE counter of the path status byte (V5, Bit 3) from each received VT superframe.

VT PTR JUST

VT Pointer Justifications — Counts the number of times the VT path pointer byte (V1 and V2) changed since initial SONET frame synchronization.

VT PTR INC

VT Pointer Increments — Counts the number of times the VT pointer bytes (V1 and V2) indicated an increment to the VT payload pointer since initial SONET frame synchronization.

VT PTR DEC

VT Pointer Decrements — Counts the number of times the VT pointer bytes (V1 and V2) indicated a decrement to the VT payload pointer since initial SONET frame synchronization.

VT PTR NDF

VT Pointer New Data Flags — Counts the number of times the VT pointer bytes (V1 and V2) indicated an active new data flag (arbitrary change in pointer) since initial SONET frame synchronization. An active NDF occurs during a change in payload content, or after an AIS or some other failure condition.

VT PTR DATA

VT Pointer Data —Presents the current VT pointer value from 0 to 103. *UNAVAILABLE* appears under a number of error conditions, such as line AIS, etc. *OUT OF RANGE* appears if the pointer value is outside 0 to 103.

13.14 ATM CATEGORY

The following test results only appear when the SONET OC-3c ATM Option is installed.

MASK CELLS

Mask Cells — Counts all cells received that match specified test mask receive addresses selected in the ATM RX auxiliary functions.

MASK CELL BW

Mask Cell Bandwidth — Measures bandwidth of the selected received profile. Select the received profile using the ATM RX-PROFILE auxiliary function.

IDLE BW

Idle Bandwidth — Measures bandwidth of all idle cells as a percentage of the received signal.

IN-USE BW

In-Use Bandwidth — Measures the active cell bandwidth as a percentage of the received signal.

BKGRD BW

Background Bandwidth — Measures the active cell traffic that does not match the selected test mask. The value is measured as a percentage of the received signal, and does not include idle cells. The test cell can be selected with the ATM RX TEST MASK auxiliary function.

MIN/MAX BW

MASK CELL

Minimum/Maximum Bandwidth — Measures highest and lowest values for the bandwidth using the selected received bandwidth period. The bandwidth period is selected through the ATM RX-BW PERIOD auxiliary function.

BURST BW

Burst Bandwidth — Measures the current bandwidth using the selected received bandwidth period. The bandwidth period is selected through the ATM RX-BW PERIOD auxiliary function.

MASK CELL RT

Mask Cell Rate — Measures the cell rate of the selected received profile in cells per second (C/s).

IDLE RT

Idle Cell Rate — Measures idle cells in cells per second (C/s).

IN-USE RT

In-Use Rate — Measures the active cells in cells per second (C/s).

BKGRD RT

Background Rate — Measures the active cell traffic that does not match the selected test mask. This value is measured in cells per second (C/s) and does not include idle cells. Select the test mask through the ATM RX-TEST MASK auxiliary function.

MIN/MAX RT

Minimum/Maximum Rate — Records the highest and lowest in-use rates during the programmed bandwidth period. Select the programmed bandwidth period through the ATM RX-BW PERIOD auxiliary function.

BURST RT

Burst Rate — Measures the current mask cell burst (in C/s) rate using the selected received bandwidth period.

MIN DLAY VAR

Minimum Cell Delay Variation — Measures minimum cell delay variation on the transmitted cell profile. The result is only available when a TTC profile is received.

MAX DLAY VAR

Maximum Cell Delay Variation — Measures maximum cell delay variation on the transmitted cell profile. The result is only available when a TTC profile is received.

AVG DLAY VAR

Average Cell Delay Variation — Measures average cell delay variation on the transmitted cell profile. The result is only available when a TTC profile is received.

TOTL CONGEST

Total Marked Congestion — Measures bandwidth of all cells marked congested as a percentage of total active cells, not including idle cells, since initial cell synchronization.

MASK CONGEST

Received Mask Cells Marked Congested — Measures bandwidth of the cells matching the receive mask which are marked congested, as a percentage of total active cells, not including idle cells, since initial cell synchronization.

% CLP=1

Percent of Cells with CLP Equals One — Measures percentage of all cells that match the selected RX mask with CLP equal to 1.

CLP=1

Cells with CLP Equals One — Counts all cells that match the selected RX mask with CLP equal to 1.

MISINSERTED

Misinserted Cells (TTC) — Counts cells that do not have the TTC payload. The result is only available when a TTC profile is received.

%MISINSERTED

Percent of Misinserted Cells (TTC) — Measures percentage of cells that do not have the TTC payload. The result is only available when a TTC profile is received.

OUT OF SEQ

Out Of Sequence TTC Sequence Number (TTC) — Counts cells that have an out of sequence TTC sequence number in the payload of the cell. The result is only available when TTC test cells are received.

% OUT OF SEQ

Percent of Out Of Sequence TTC Sequence Number (TTC) — Measures percentage of cells that have an out of sequence TTC sequence number in the payload of the cell. The result is only available when TTC test cells are received.

DROP'D CELLS

Dropped Received Mask Cells (TTC) — Counts the dropped RX Mask Cells. The result is only available when TTC test cells are received.

% DROP'D

Percent of Dropped Received Mask Cells (TTC) — Measures percentage of dropped RX Mask Cells. The result is only available when TTC test cells are received.

HEC ERRORS

Header Error Control Errors — Counts all cells with at least one HEC error.

HEC ERR RATE

Header Error Control Error Rate — Counts the ratio of HEC errors over the total number of received cells.

CORRECT ERRS

Correctable HEC Errors — Counts the cells with only one HEC error. If a cell with a single HEC error is followed by consecutive cells that have one or more HEC errors, then only the first HEC errored cell is counted as correctable.

CORRECT RATE

Correctable HEC Error Rate — Counts the ratio of correctable errors over the total number of received cells.

NON-COR ERRS

Non-Correctable HEC Errors — Counts cells with more than one HEC error. Also the count of consecutive cells that have HEC errors excluding the first cell, if and only if, it has a single HEC error.

NON-COR RATE

Non-Correctable HEC Error Rate — Counts the ratio of non-correctable errors over the total number of received cells.

CORR TAG

Correlation Tag (TTC) — Indicates the current received TTC cell correlation tag number. The result is only available when a TTC profile is received.

AIS SECONDS

AIS Alarm Seconds — Counts the seconds an ATM AIS alarm is detected since the last test restart or history reset.

RDI SECONDS

RDI Alarm Seconds —Counts the seconds an ATM RDI alarm is detected since the last test restart or history reset.

CSF SECONDS

Cell Synchronization Failure Seconds — Counts number of cell synchronization failure seconds detected.

ATM STATUS

ATM Status Results, Summary Category — Displays the following ATM signal status conditions as they occur:

CELL SYNC — Cell Synchronization indicates the reception of six consecutive unerrored HECs. This is equivalent to a cell delineation (CD) indication.

OUT OF SYNC — Out of Synchronization — Indicates the reception of at least seven consecutive errored HECs after cell synchronization. This is equivalent to an out of cell delineation (OCD).

SYNC LOSS — Loss of Synchronization — Indicates continued loss of cell synchronization 4 ms after out of synchronization occurred. This is equivalent to a loss of cell delineation (LCD) indication.

SYNC FAILURE — Synchronization Failure — Indicates synchronization loss is present for 2.5 seconds. Cleared when cell synchronization is regained and loss of synchronization has not occurred in 10 seconds. This is equivalent to a loss of cell delineation failure (LCD FAILURE) indication.

DS1/DS0 TEST
RESULTS

DS1/DS0 ANALYZER TEST RESULTS

14.1 SIGNAL STATUS LED DEFINITIONS

The following green Status LEDs provide information about the condition of the received DS1 signal. The Status LEDs are described as follows:

T1 Pulses — Illuminates when the 310-1 detects multiple T1 pulses from one of three DS1 sources: the side-panel DS1 RECEIVE jack, channelized DS3, or SONET DS1 payload. If the received signal is lost, the LED goes out and the Signal Loss LED illuminates.

Frame Sync — Illuminates when the 310-1 acquires frame synchronization. If the received framing format is lost, the LED goes out and the Frame Loss LED illuminates.

Pattern Sync — Illuminates when the 310-1 synchronizes to the test pattern displayed in the PATTERN window. If pattern synchronization is lost, the LED goes out and the Pattern Loss LED illuminates.

B8ZS — Illuminates when B8ZS clear channel coding is detected in the received DS1 signal. When B8ZS encoding is detected and the **CODE** switch is set to AMI, the message *B8ZS DETECTED* is also displayed in the SUMMARY category. The LED is only active when the **DS1 SOURCE** switch is set to EXT. INPUT (side-panel DS1 RECEIVE jack).

14.2 SIGNAL ALARM LED DEFINITIONS

The red Alarm LEDs provide information about the current and historical alarm conditions related to the received signal. These LEDs are divided into two columns (current and history). The right column illuminates when an alarm condition occurs and remains illuminated as long as the alarm exists. When the current alarm condition is cleared (e.g., pattern sync reestablished), its History LED illuminates. The History LEDs indicate past occurrences of the alarm and remain illuminated until either the **HISTORY RESET** switch is pressed or a 310-1 test restart occurs. The Alarm LEDs are described as follows:

Signal Loss — Illuminates when no pulses are detected. When T1 pulses are detected again, the Alarm LED goes out, and its History LED and the T1 Pulses LED illuminate.

Frame Loss — Illuminates when frame synchronization is lost. When DS1 framing is detected again, the Alarm LED goes out, and its History LED and the Frame Sync LED illuminate.

Pattern Loss — Illuminates when pattern synchronization is lost. When the pattern is resynchronized, the Alarm LED goes out, and its History LED and Pattern Sync LED illuminate.

Excess Zeros — Illuminates when excess zeros are detected in AMI or B8ZS coding. When excess zeros are no longer detected, the LED goes out and its History LED illuminates. The LED is only active when the DS1 SOURCE switch is set to EXT. INPUT.

Yellow Alarm — Illuminates when a Yellow Alarm is detected. When the Yellow Alarm is no longer detected, the LED goes out and its History LED illuminates.

All Ones — Illuminates when all ones are detected in framed and unframed DS1 signals. When All Ones are no longer detected, the LED goes out and its History LED illuminates.

HISTORY RESET switch — This switch clears all History LEDs on the 310-1. This switch does not restart a test, or affects any of the Alarm LEDs or accumulated results. It is not operable when the **DISPLAY HOLD** switch is activated. The **RESTART** switch also clears the History LEDs.

14.3 SUMMARY CATEGORY

When all SUMMARY results are error-free, the message *ALL RESULTS OK* is displayed. When an error is detected, the appropriate test result appears in the SUMMARY category window (the results are identified in the following sections). If no signal is detected, the message *ALL RESULTS UNAVAILABLE* appears in the display. When more than one error is detected, press either the **RESULTS I Results** switch or **RESULTS II Results** switch to scroll through the results. The results that appear in the SUMMARY category include:

- BIT ERRORS (LOGIC category)
- FRM ERRORS (FRAME category)
- SLIPS (LOGIC category)
- CRC ERRORS (FRAME category)
- VIOLATIONS (BPV category)
- RX FREQ (SIGNAL category)

14.3.1 310-9A/B Option PRM Test Results

When the 310-9A/B option is installed and the PRM results are enabled, the following results can appear in the SUMMARY category. It should be noted that these results apply to the far-end received signal.

- FAR BPV SEC (BPV category)
- FAR FRM ES (FRAME category)
- FAR FRM SES (FRAME category)
- FAR SLIP SEC (FRAME category)
- FAR CRC ERR (FRAME category)

The optional ESF datalink far-end Performance Report Message (PRM) results enable the DS1/DS0 Analyzer Option to monitor and report on the status of the ESF PRM as described in the ANSI T1.403-1989 standard. The far-end PRM results are available when the ESF or optional ESFz operating mode is selected and the AUX-PRM receiver auxiliary function is enabled. The AUX-PRM auxiliary function determines whether the following PRM results are reported.

BPV Category
- FAR BPV SEC — Far-End BPV Seconds

FRAME Category
- FAR FRM ES — Far-End Frame Error Seconds
- FAR FRM SES — Far-End Severely Errored Framing Seconds
- FAR SLIP SEC — Far-End Controlled Slip Seconds
- PAYLOAD SOURCE — Far-End Payload Source/Loopback
- FAR CRC ERR — Far-End CRC Error Events
- FCRC 1 — Far-End CRC 1 Bin
- FCRC 2-5 — Far-End CRC 2 to 5 Bin
- FCRC 6-10 — Far-End CRC 6 to 10 Bin
- FCRC 11-100 — Far-End CRC 11 to 100 Bin
- FCRC 101-319 — Far-End CRC 101 to 319 Bin
- FCRC >319 — Far-End CRC 320 to 333 Bin

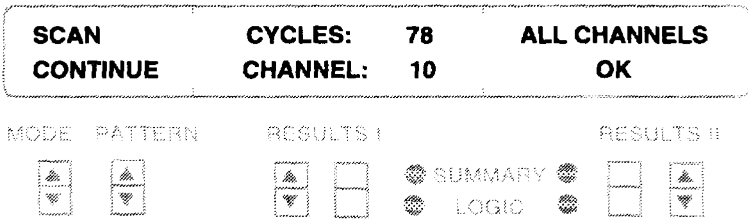
TIME Category
- FAR PRM SEC — Far-End Performance Report Seconds

When a far-end PRM result count is an approximation because of a lost PRM, a "~" (tilde) precedes the result. The results are halted when the frame synchronization or the signal is lost during testing. When the FAR CRC ERR result is displayed and the indicated count is an approximation of the actual CRC error count, a ">" (greater than) sign precedes the count.

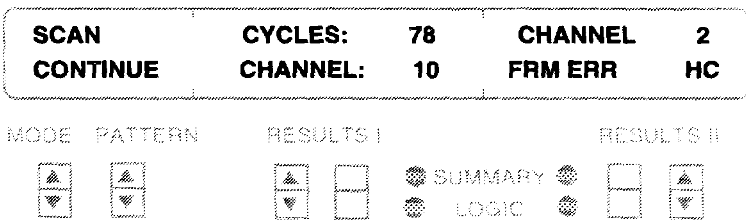
14.3.2 310-9A/B Option SCAN Mode Test Results

When the DS1/DS0 Analyzer Option is configured in SCAN mode, the results appear according to the selected SCAN mode: CONTINUE or TRIGGER.

SCAN CONTINUE — In the continuous DS1 scan mode, the RESULTS I window displays the CYCLE and CHANNEL results. The CYCLE result indicates the number of times the scan has cycled completely through all the DS1 channels. The CHANNEL number result indicates the channel which is currently being scanned. The RESULTS II window displays the status messages, alarms, or errors. If the dropped DS1 channels are error free, the message *ALL CHANNELS OK* appears.



When an error or alarm is detected, the channel number and error appear in the RESULTS II window.



An **H** or **C** appears next the to test result indicating the error status as *History* or *Current*. The following errors or alarms are detectable:

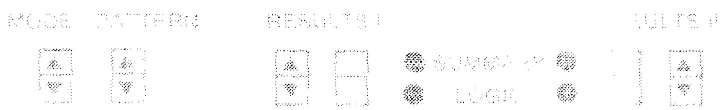
CRC ERRORS — Cyclic Redundancy Check Errors
FRM ERRORS — Frame Errors
SLIPS — Timing Slips (requires the 310-9A/B option and a reference signal source)
ALL ONES — All Ones Pattern
YELLOW — Yellow Alarm
FRM LOSS— Frame Synchronization Loss

SCAN TRIGGER — In SCAN TRIGGER mode the RESULTS I window displays the CYCLE and CHANNEL results. The CYCLE result indicates the number of times the scan has cycled completely through all the DS1 channels. The CHANNEL number result indicates the channel which is currently being scanned. The RESULTS II window displays test status messages.

SCAN	CYCLES:	78	SEARCHING FOR
TRIGGER	CHANNEL:	10	TRIGGER EVENT

If the scan detects a selected event from the AUX-SCAN TRIG auxiliary function, the DS1/DS0 Analyzer Option stops scanning and automatically configures to the dropped channel. A leading asterisk (*), framing format, and pattern appear in lowercase characters in the MODE/PATTERN window. When an event is detected, scanning stops and full DS1 logic, BPV, CRC, frame, and signal error analysis is performed. The LOGIC category is not applicable during live data analysis. The RESULTS I and II windows provide BERT analysis results.

*t1 slc	BIT ERRORS	FRM ERRORS
*qrss	786	2



14.4 LOGIC CATEGORY

NOTE: If "N/A" appears in the display, the result does not apply to the current test configuration.

14.4.1 DS1 Test Results

BIT ERRORS

Bit Errors — The number of received pattern bits which have a value opposite that of the corresponding transmitted bit pattern since initial DS1 pattern synchronization. The result also appears in the SUMMARY category (count > 0).

BIT ERR RT

Bit Error Rate — The ratio of pattern bit errors to received pattern bits since initially acquiring pattern synchronization.

ASYNC ERR SEC

Asynchronous Errored Seconds — The number of seconds during which one or more pattern bit errors occurred since initial DS1 pattern synchronization.

SYNC ERR SEC

Synchronous Errored Seconds — The number of seconds during which at least one pattern bit error has occurred. Each second is initiated by, and synchronized to, a pattern bit error.

%EFS

Bit, Percentage of Error-Free Seconds — The ratio, expressed as a percentage, of seconds during which no pattern bit errors were detected to the total number of seconds while DS1 pattern synchronization is present.

SYNC L SEC

Out-of-Synchronization Seconds — The number of seconds during which the receiver has lost pattern synchronization, even momentarily, since initial DS1 pattern synchronization.

SEV ERR SEC

Severely Errored Seconds — The number of seconds during which the pattern bit error rate exceeded or equaled 10^{-3} b/s.

CSES

Consecutive Severely Errored Seconds—The number of groups of three or more severely errored seconds.

SLIPS

Slips — The number of times the received pattern becomes skewed relative to the expected (i.e., internally generated) test pattern. When a slip is detected, the 310-1 automatically resynchronizes to the received pattern. However, pattern bit errors are not suppressed during this process. Pattern slips are available only when using pseudorandom patterns. The result also appears in the SUMMARY category (count > 0).

14.4.2 G.821 Results Option Test Results

AVAIL SEC

Available Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is less than 10^{-3}.

%AVAIL SEC

% Available Seconds — The ratio, expressed as a percentage, of available seconds to the total elapsed seconds since pattern synchronization.

%SEV ER SEC

% Severely Errored Seconds — The ratio, expressed as a percentage, of severely errored seconds to the number of available seconds.

DEG MIN

Degraded Minutes — A count of minutes during which the bit error ratio is worse than 10^{-6} and less than 10^{-3}.

%DEG MIN

% Degraded Minutes — The ratio, expressed as a percentage, of degraded minutes to the number of available minutes.

UNAVAIL SEC

Unavailable Seconds — A count of elapsed seconds since pattern synchronization in which the bit error rate is greater than or equal to 10^{-3}.

14.5 BPV CATEGORY

VIOLATIONS

Bipolar Violations — The number of bipolar violations (BPVs) detected since the beginning of the test. Intentional B8ZS code violations are excluded from the count. The result also appears in the SUMMARY category (count > 0).

BPV ERR RT

BPV Error Rate — The ratio of BPVs to received bits since initially acquiring signal presence.

BPV ERR SEC

BPV Errored Seconds — The number of seconds during which one or more BPVs occurred since the beginning of the test.

FAR BPV SEC

Far-End BPV Seconds — The number of seconds during which one or more BPVs occurred in the far-end received signal. This result reports on the PRM Line-Code Violation Event Bit (LV = 1) status. This result requires the 310-9A Enhanced ESF/ DS1 Timing Slips Option or the 310-9B Enhanced DS1 Testing Option.

14.6 FRAME CATEGORY

14.6.1 DS1 Frame Test Results

FRM ERRORS

Frame Errors—The number of frame errors detected since initial DS1 frame synchronization.

FRM ERR RT

Frame Error Rate—The ratio of frame errors to received framing bits since initially acquiring frame synchronization.

FRM ERR SEC

Frame Errored Seconds—The number of seconds during which one or more frame errors occurred since initial DS1 frame synchronization.

FRM SES

Frame Severely Errored Seconds — The number of seconds during which the total number of frame errors equals 12 or more (D4 framing only).

FRM L SEC

Frame Loss Seconds — The number of seconds during which one or more frame synchronization losses occurred or during which frame synchronization could not be achieved, since initial DS1 frame synchronization.

CRC ERRORS

Cyclic Redundancy Check Errors—The number of CRC errors detected since initial DS1 frame synchronization. CRC errors are counted only when ESF or ESFz framing is present in the received T1 data.

CRC ERR SEC

Cyclic Redundancy Check Errored Seconds—The number of seconds during which one or more CRC errors occurred.

CRC ERR RT

Cyclic Redundancy Check Error Rate — The ratio of CRC errors to the number of superframes received.

CRC SES

Cyclic Redundancy Check Severely Errored Seconds — The number of seconds during which the total number of CRC errors and frame synchronization losses equaled 320 or more.

14.6.2 310-9A/B Option PRM Test Results

FAR FRM ES

Far-End Frame Error Seconds — The number of seconds during which one or more frame errors occurred in the far-end received signal. This result reports on the PRM Frame-Synchronization-Bit Error Event Bit (FE = 1) status.

FAR FRM SES

Far-End Severely Errored Framing Seconds — The number of seconds during which two or more frame errors occurred in less than 3 ms in the far-end received signal. This result reports on the PRM Severely-Errored Framing Event Bit (SE = 1) status.

FAR SLIP SEC

Far-End Controlled Slip Seconds — The number of seconds during which controlled slips occurred in the far-end received signal. This result reports on the PRM Controlled-Slip Event Bit (SL = 1) status.

PAYLOAD SOURCE

Far-End Payload Source/Loopback — Identifies the direction of the PRM according to the PRM Command/Response Bit (C/R) and the Payload Loopback Activated Bit (LB). In end-to-end applications, a customer-generated PRM is indicated as CUST (C/R = 0 and LB = 0), and the carrier-generated PRM is indicated as CARR (C/R =1 and LB = 0) in the display. In payload loopback applications, the customer-generated PRM is indicated as CUST LOOP (C/R = 0 and LB = 1) when the customer is looped back, and the carrier-generated PRM is indicated as CARR LOOP (C/R = 1 and LB = 1) when the carrier is looped back.

FAR CRC ERR

Far-End CRC Error Events — The minimum number of CRC errors reported in the following FCRC results. A">" (greater than) preceding the count indicates the Bins 2 through 6 are non-zero. This result reports on the PRM CRC Error Event Bits (G1 to G6) status.

VF LVL dBm
Received Signal Level in dBm — The level of the average power

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14.5 BPV CATEGORY

VIOLATIONS

Bipolar Violations — The number of bipolar violations (BPVs) detected since the beginning of the test. Intentional B8ZS code violations are excluded from the count. The result also appears in the SUMMARY category (count > 0).

BPV ERR RT

BPV Error Rate — The ratio of BPVs to received bits since initially acquiring signal presence.

BPV ERR SEC

BPV Errored Seconds — The number of seconds during which one or more BPVs occurred since the beginning of the test.

FAR BPV SEC

Far-End BPV Seconds — The number of seconds during which one or more BPVs occurred in the far-end received signal. This result reports on the PRM Line-Code Violation Event Bit (LV = 1) status. This result requires the 310-9A Enhanced ESF/ DS1 Timing Slips Option or the 310-9B Enhanced DS1 Testing Option.

14.6 FRAME CATEGORY

14.6.1 DS1 Frame Test Results

FRM ERRORS

Frame Errors—The number of frame errors detected since initial DS1 frame synchronization.

FRM ERR RT

Frame Error Rate—The ratio of frame errors to received framing bits since initially acquiring frame synchronization.

FRM ERR SEC

Frame Errored Seconds—The number of seconds during which one or more frame errors occurred since initial DS1 frame synchronization.

FRM SES

Frame Severely Errored Seconds — The number of seconds during which the total number of frame errors equals 12 or more (D4 framing only).

FRM L SEC

Frame Loss Seconds — The number of seconds during which one or more frame synchronization losses occurred or during which frame synchronization could not be achieved, since initial DS1 frame synchronization.

CRC ERRORS

Cyclic Redundancy Check Errors— The number of CRC errors detected since initial DS1 frame synchronization. CRC errors are counted only when ESF or ESFz framing is present in the received T1 data.

CRC ERR SEC

Cyclic Redundancy Check Errored Seconds— The number of seconds during which one or more CRC errors occurred.

CRC ERR RT

Cyclic Redundancy Check Error Rate – The ratio of CRC errors to the number of superframes received.

CRC SES

Cyclic Redundancy Check Severely Errored Seconds — The number of seconds during which the total number of CRC errors and frame synchronization losses equaled 320 or more.

14.6.2 310-9A/B Option PRM Test Results

FAR FRM ES

Far-End Frame Error Seconds — The number of seconds during which one or more frame errors occurred in the far-end received signal. This result reports on the PRM Frame-Synchronization-Bit Error Event Bit (FE = 1) status.

FAR FRM SES

Far-End Severely Errored Framing Seconds — The number of seconds during which two or more frame errors occurred in less than 3 ms in the far-end received signal. This result reports on the PRM Severely-Errored Framing Event Bit (SE = 1) status.

FAR SLIP SEC

Far-End Controlled Slip Seconds — The number of seconds during which controlled slips occurred in the far-end received signal. This result reports on the PRM Controlled-Slip Event Bit (SL = 1) status.

PAYLOAD SOURCE

Far-End Payload Source/Loopback — Identifies the direction of the PRM according to the PRM Command/Response Bit (C/R) and the Payload Loopback Activated Bit (LB). In end-to-end applications, a customer-generated PRM is indicated as CUST (C/R = 0 and LB = 0), and the carrier-generated PRM is indicated as CARR (C/R =1 and LB = 0) in the display. In payload loopback applications, the customer-generated PRM is indicated as CUST LOOP (C/R = 0 and LB = 1) when the customer is looped back, and the carrier-generated PRM is indicated as CARR LOOP (C/R = 1 and LB = 1) when the carrier is looped back.

FAR CRC ERR

Far-End CRC Error Events — The minimum number of CRC errors reported in the following FCRC results. A">" (greater than) preceding the count indicates the Bins 2 through 6 are non-zero. This result reports on the PRM CRC Error Event Bits (G1 to G6) status.

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14.8 TIME CATEGORY

TIME

Current Time of Day— The current time of day in hours, minutes, and seconds. The time is set through the TIME-SET TIME mainframe function.

DATE

Current Date — The current day and month. The date is set through the TIME-SET DATE mainframe function.

ELAPSED TIME

Elapsed Time— The elapsed time in hours, minutes, and seconds since the last 310-1 test restart. If there is no DS1 signal present after test restart the test does not begin.

TEST LENGTH

Timed Test Length — The currently set test length for a timed test in hours and minutes on the 310-1. The test length is set through the TIME-TEST LENGTH mainframe auxiliary function. If the mainframe **TIME-TEST** auxiliary function is set to CONTINUOUS, this result is N/A.

TIME LEFT

Timed Test Time Left —The time remaining for a timed test in hours, minutes, and seconds on the 310-1. If the mainframe **TIME-TEST** auxiliary function is set to CONTINUOUS, this result is N/A.

FAR PRM SEC

Far-End Performance Report Seconds — The number of total seconds, since test restart, during which a valid PRM was received. Requires the 310-9B Enhanced DS1 Testing Option or the 310-9A Enhanced ESF/Timing Slips Option.

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